

**LOW COST ACTIVE CLAMP FOR HIGH FREQUENCY APPLICATIONS**

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**INTRODUCTION**

Purpose of this application is to describe a single-switch forward converter with two outputs, 5V-20A and 12V-4A, with an active clamp system. This is an application close to Personal Computer and logic cards power supplies. For the approached output power level, 150W, the single transistor forward converter represents, in addition to the high frequency operation, the best solution. Moreover, with the help of the active clamp, it is possible to break the 50% duty cycle barrier, typical of this topology, reaching in some cases the 70% of max. duty cycle.

**TOPOLOGY OVERVIEW**

The single switch forward converter requires a circuitry that allows to recirculate the magnetizing current and discharging the leakage inductance energy. The main traditional solutions are :

- Auxiliary winding
- RCD clamp

The first method requires a tertiary winding, with a calculated number of turns to clamp the re-

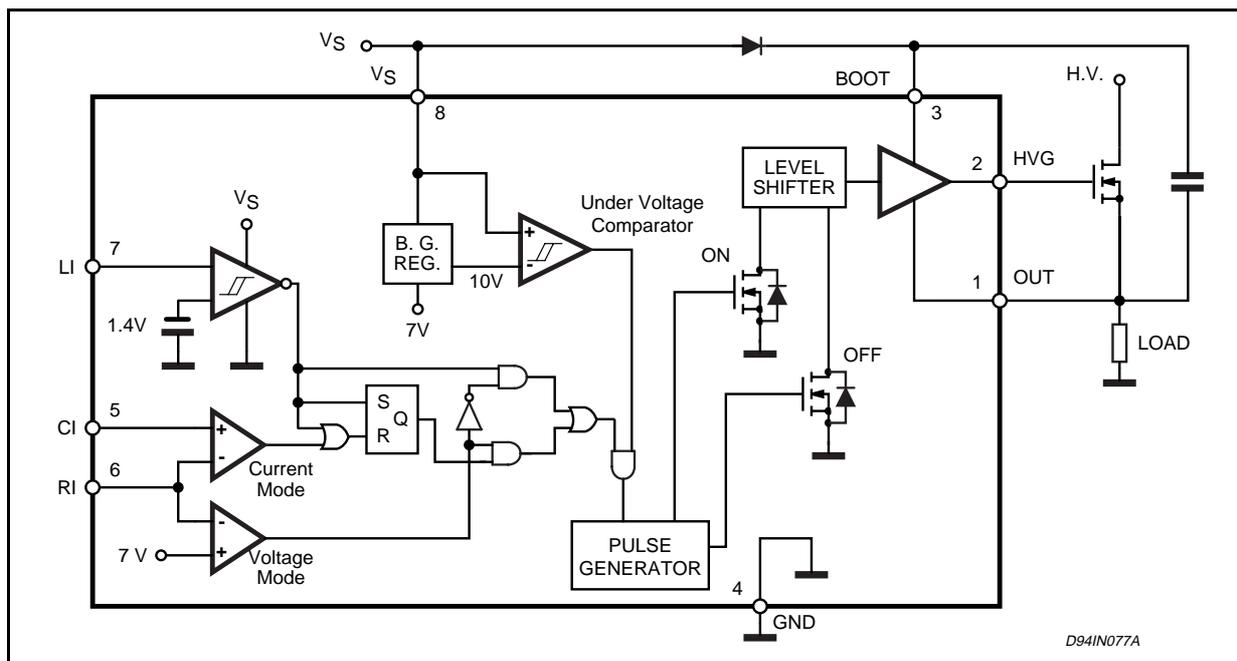
flected secondary to primary voltage at a safety value; this winding allows to discharge the magnetizing current to reset the core, and it has to be realized very well coupled to the primary winding. An ultrafast high voltage diode is requested too. The second method is a dissipative clamp, with power losses proportional to the switching frequency. An innovative clamp solution, usually called "active clamp" permits to recirculate the magnetizing current and leakage inductance energy with much less EMI problems and reduced turn-on power Mos switching losses.

This topology is realized by a high voltage level shifter driver, driving a source floating power Mos transistor, with the clamp capacitance in series to the drain. A level shifter, L6380, allows to realize a low cost solution capable to work at the requested switching frequency, with an easy implementation of the delay times for the correct functionality of this topology. This device is composed of:

- floating p-kefet up to 600V, in which is allocated the high side driver with low voltage components
- logic inputs referred to ground

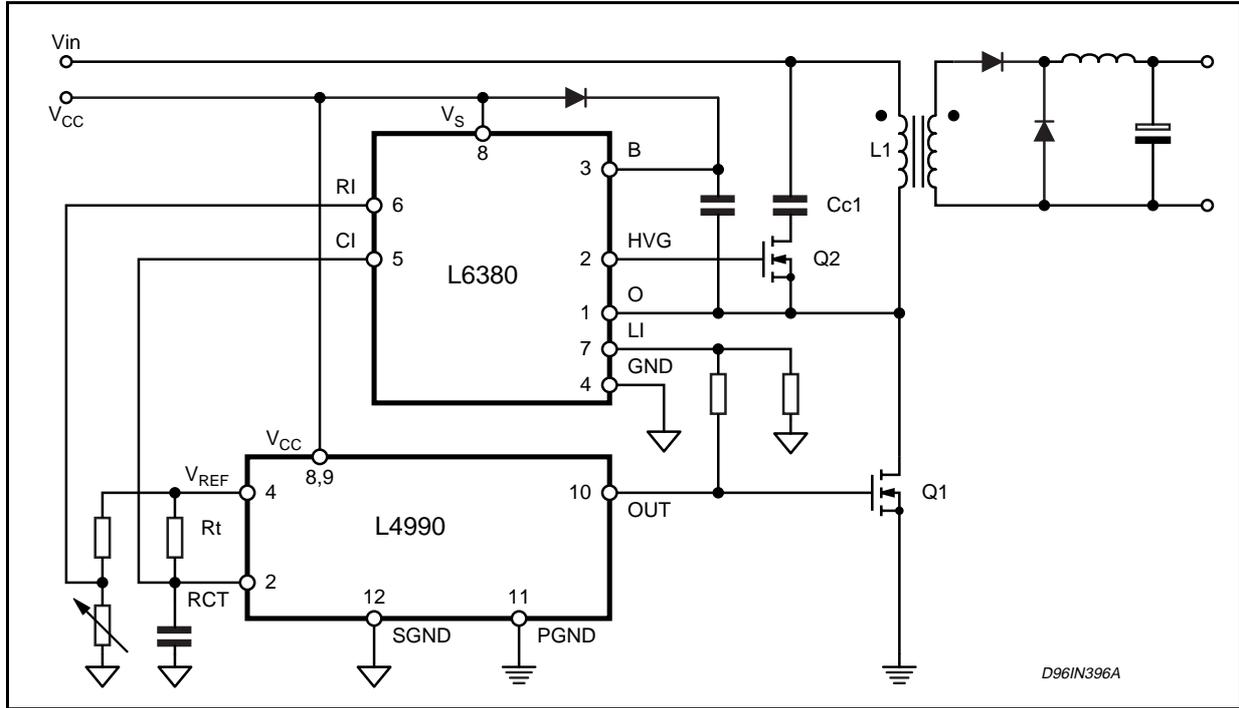
In Fig 1 is shown the L6380 block diagram.

**Figure 1:** L6380 level-shifter block diagram.



# APPLICATION NOTE

**Figure 2a:** Active Clamp Basic Schematic.



**Figure 2b:** System Waveforms.

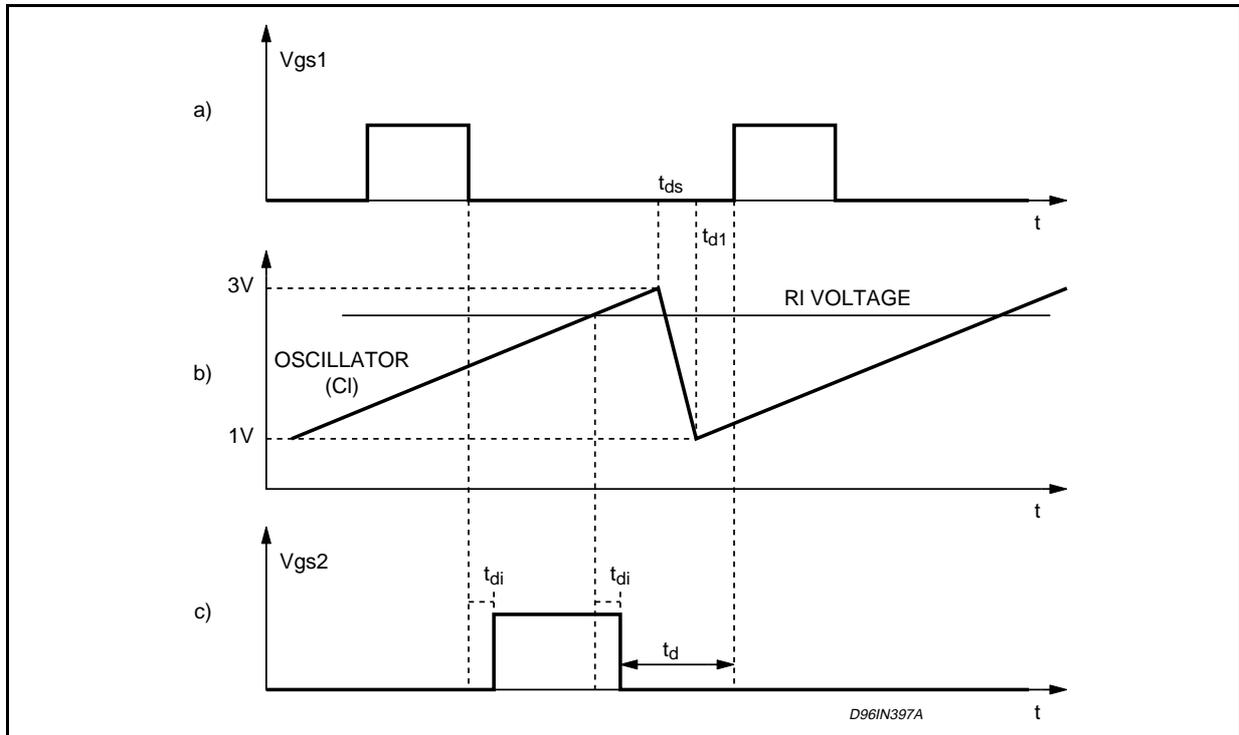


Fig 2a shows the connection of the level shifter with the PWM controller, and fig 2b shows the L4990 oscillator with gate voltage waveforms of

the two transistors. The high voltage level shifter eliminates the need of the gate drive transformer reducing the number of magnetic components and cost.

**SYSTEM DESCRIPTION**

The programming delay time ( $t_d$ ) between the Q2 turn-off and the Q1 turn-on is realized with the help of a voltage divider of the PWM controller reference voltage. The delay time allows to turn-on the power mos at the moment where the resonance voltage waveform reaches the valley. The resonance is generated between the primary inductance and the mos (Q1) output capacitance,  $C_{oss}$ . The resulting drain voltage is lower than the supply voltage at the turn-on. This delay must be a quarter of the resonant period. It is possible to evaluate the voltage at pin RI that produces the desired delay time using the equation:

$$V_{RI} = 3 - \frac{2}{t - t_{ds}} \cdot (t_d + t_{di} - t_{d1} - t_{ds}) \quad \text{Eq 1}$$

This equation is calculated fixing the oscillator capacitor at 1nF. Fig3 is the graphical representation of this equation, for different switching frequencies.

The connections between level shifter and L4990 are possible and simple because the pwm controller can program the maximum duty cycle without touching the discharge time of the oscillator. The clamp capacitance value,  $C_c$  is:

$$C_c = \frac{1}{L_p} \cdot \left( \frac{6}{2 \cdot \pi \cdot F_{sw}} \right)^2 \quad \text{Eq2}$$

This is an approximate value, calculated considering the primary inductance-clamp capacitance resonance period as 6 times the switching period. This method does not consider the ripple voltage on the capacitance [1].

**POWER SUPPLY DESCRIPTION**

**Power Supply Specification**

Input Voltage: 220Vac (176Vac to 265Vac) @ 50Hz  
 110Vac ( 88 Vac to 132 Vac) @ 60Hz  
 (manually selectable)

Output 1: 5V - 20A (<1% ripple)  
 Output 2: 12V - 4A  
 Switching Frequency: 300kHz  
 Target Efficiency (full load)> 80%  
 Dmax: 45%

**Power Transformer Design,T1**

The transformer core selected for this application is the ETD39, 3F3, material particularly intended for high frequency operation. The total transformer losses are fixed at 1.5% of the total output power (about 2.2W in total, 1.1W copper losses and 1.1W core losses). The primary and secondary numbers of turns are calculated considering 174V of minimum DC input voltage and 80mT of max.  $\Delta B$  :

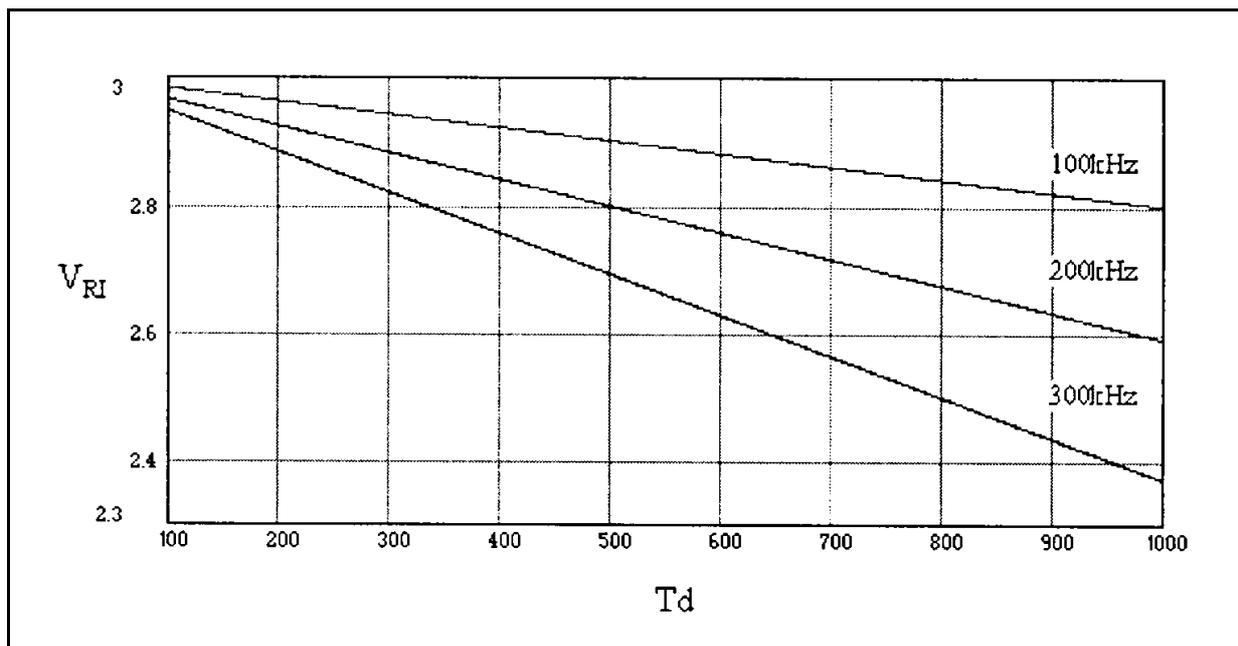
$$N_p = 34T \quad N_{s5V} = 3T \quad N_{s12V} = 4T$$

The copper losses are fixed at 550mW for the primary, and at 225mW for each secondary. Litz wire has been chosen for minimising the skin effect:

- Windings:
- Primary: 1 Litz of 60 wires
- Secondary 5V: 4 Litz of 90 wires
- Secondary 12V: 1 Litz of 60 wires

The obtained primary inductance is 3mH, and the magnetizing current is 90mA max.. The primary peak current is 2.36 A corresponding at an RMS current of 1.6A.

**Figure 3:** RI voltage vs delay time, at various switching frequencies.



## APPLICATION NOTE

### Output inductor, L4

In multioutputs forward converters it is common practice to couple the output inductors using one single core with multiple windings; this technique reduces cost, space and improves regulation.

The inductor windings have be calculated according to the transformer turns ratio of the relatives secondary windings for optimum regulation and stability.

The multichoke is realized with the 77930 kool- $\mu$  core; 6T (4 $\mu$ H) are required for the 5V output, and 8T for the 12V output, according to the transformer turns ratio. The current ripple on the 5V output is limited at about 3A, less than 15% of max. output current. For the 5V and 12V windings 18wires of 0.4mm(AWG26) and 1 wire of 1mm(AWG18) have been used. Power dissipation at max. load is about 4W and the temperature rise is 54°C.

### Output Capacitors

For the 5V output, the ripple voltage is limited at 1% max.. The output total ESR capacitance has to be lower than 16mohm considering the 3A of ripple current. Three capacitors of 1500 $\mu$ F/10V LXF (NCC) with an ESR of 44 mohm each satisfy the specification requirements. However, the output capacitor have been decoupled by one small inductor, L6, to minimize the ripple voltage and switching spikes.

### Input Capacitors

The ac mains is manually selectable and in case of 110Vac the input capacitor are connected in series, for doubling the mains. The two capacitors have a value of 330 $\mu$ F/200V - KMH - NCC. The peak current is 6A, while the rms value is 2.2A.

### Power mos

In active clamp systems the reset voltage is lower than the RCD clamping voltage value. Due to this reason, Q1 has been chosen with a max. Vdss of 600V. The type is STP5NA60, having an Rds(on) of 1.5ohm max. at 25°C and a Coss of 170pF max. The rms current flowing through Q1 at maximum load and minimum supply voltage is 1.6A and the conduction losses are about 3.7W.

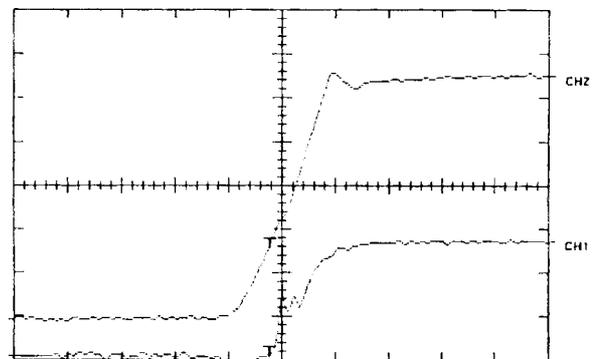
### Comparison with RCD clamping network

An RCD clamping network is designed considering the power dissipation of the resistor due to the magnetizing and leakage inductance energies. The realized transformer prototype is showing a leakage inductance of 6 $\mu$ H at 300kHz and the max. losses across the resistor is estimated around 7.8W (with R=10k and Cc=10nF).

## EXPERIMENTAL RESULTS

Experimental analisys have been performed on a bench using the prototype realized with a double side pcb. A comparison with a standard RCD clamp has been performed too, making the modification directly on the same pcb. The results are shown here below this paragraph. The real advantages of the active clamp solution are not only represented by the lower value of Vdss at which Q1 turns-on, but also by the conduction start time of the forward secondary diode that anticipate the Q1 turn-on time. In fact, when the floating mos, Q2, turns- off, the current in the primary winding cannot change the sense, and the voltage across the primary of the transformer changes the polarity, directly biasing the secondary diode D3. The current flowing into the primary winding starts to discharge the Q1 Coss reducing its voltage value. The associated energy is delivered to the secondary. Fig 4 shows the current in the forward diode and Q1 gate voltage; it is also possible to see that the current increase before Q1 turn on. Efficiency comparisons between active and dissipating clamps are reported in Fig 5, for two differents DC input voltage 240VDC and 330VDC.

**Figure 4:** CH1: Main Mos gate signal (5V/div)  
CH2: Secondary forward diode current (400mA/div)  
Time: 100ns/div



The trace called "Active 1" shows an improvement due to the introduction of a 0.2mm air gap located on the central core leg. Fig6a shows current and voltage clamp capacitance. The current waveform is composed of a first peak due to the leakage inductance energy and of a second linear portion generated by the resonance between the clamping capacitance and the primary inductance. Fig6b shows Q1 drain voltage waveforms for different air gap thickness. Increasing the air gap, Q1 turns-on at a lower drain-source voltage and the efficiency goes up.

Figure 5: Efficiencies versus output power, with different clamping networks (Active, using air Gap 0.2mm).

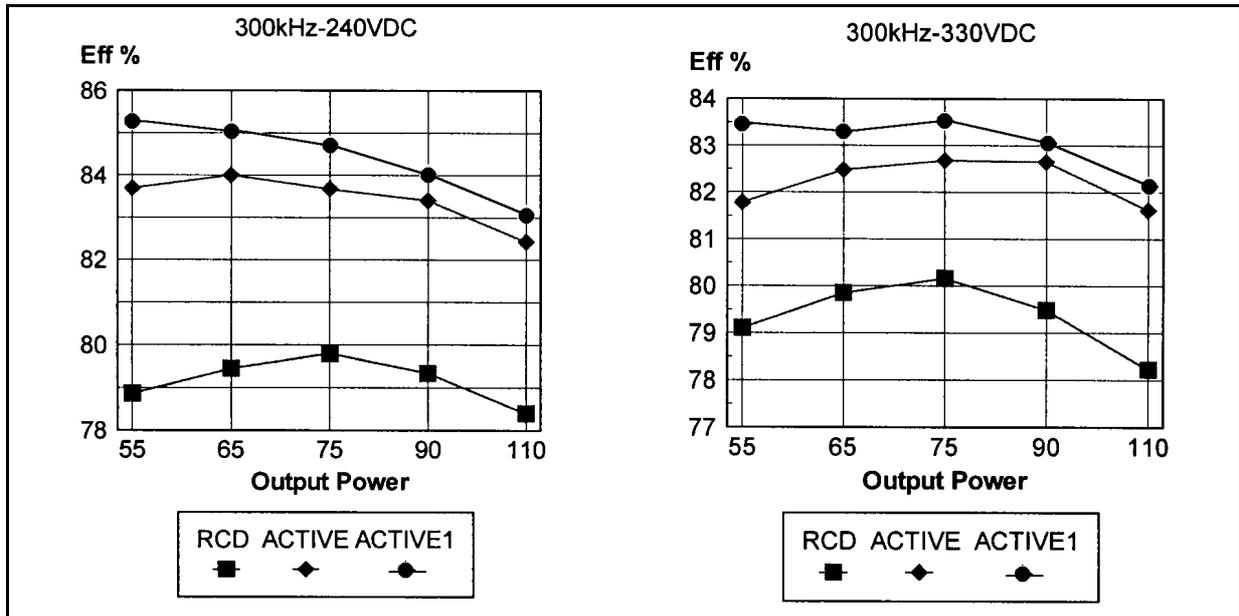


Figure 6a: CH1: Clamp Cap. Voltage (20V/div)  
CH2: Clamp Cap. Current (0.2A/div)  
Time: 500ns/div

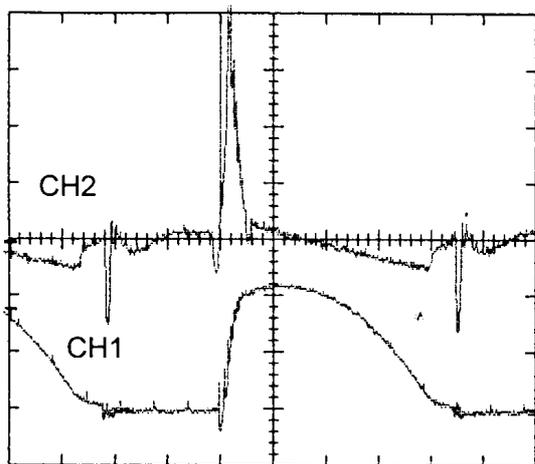


Figure 6b: Drain Voltage for different air-gap  
50V/div - 500ns/div

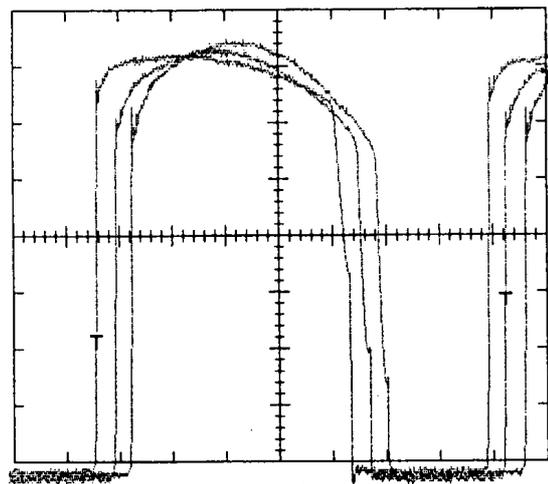


Fig 7 shows the schematic diagram of the complete application.

The primary start-up circuit has a low quiescent current and the auxiliary supply is realized with an additional primary winding forward coupled with

the main primary winding.

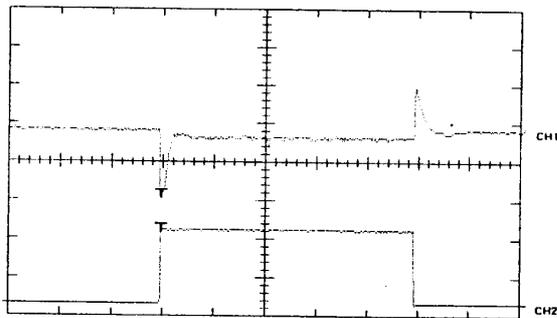
The voltage feedback loop, realized with an optoisolator and a TL431, is sensing the 5V output.

The 12V output, for a much superior precision and stability, has been post-regulated with a



very low-drop linear regulator, L4955, having an N-channel mos as pass series element, instead of a lower performant pnp bipolar transistor.

**Figure 8:** Load transient response times.  
 CH1: Output voltage (100mV/div)  
 CH2: Output current (5A/div)  
 Time: 2ms/div



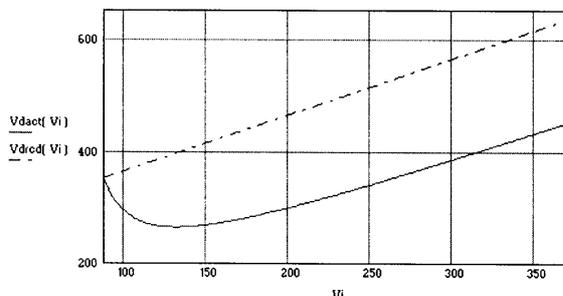
Furtherly, the active clamp system allows a reduction of the necessary  $V_{dss}$  in autoranging applications respect the solutions using the standard dissipating RCD clamp. In fact, for an input voltage ranging from 85V to 265Vac and for a 75% of max. duty cycle, the reset voltage in the case of an active clamp is significantly lower than the alternative RCD clamp solution. Equations 3 and 4 allow us to calculate the  $V_{dss}$  drain voltage with active and with RCD clamp respectively.

$$V_{dact} = \frac{V_{in\ min} \cdot D_{max}}{1 - \frac{V_{in\ min} \cdot D_{max}}{V_{in}}} + V_{in} \quad Eq3$$

$$V_{drcd} = \frac{V_{in\ min} \cdot D_{max}}{1 - D_{max}} + V_{in} \quad Eq4$$

The grafical representation of these two equations are reported in fig 9. In RCD clamp Q1 is requested to sustain a  $V_{dss}$  of 700V, while for the active clamp solution 500V are enough.

**Figure 9:** Q1  $V_{dss}$  vs dc supply voltage.



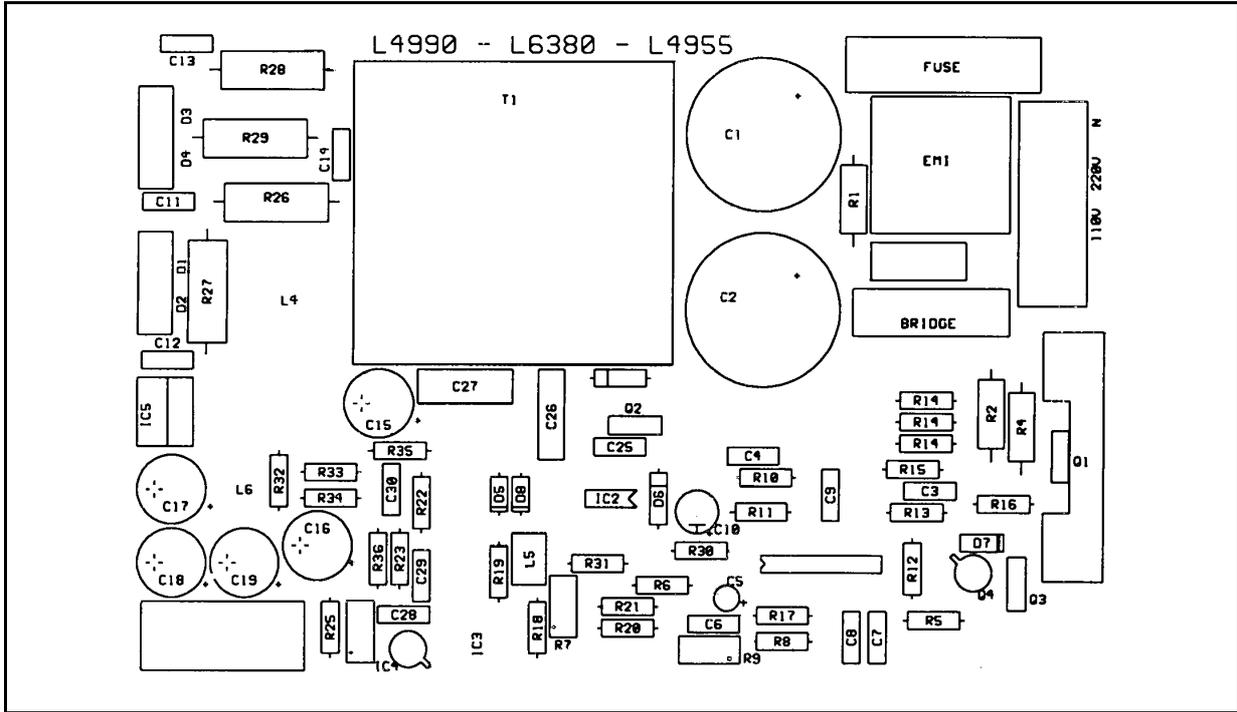
**Component List**

R1	220k 1/2W	C1	300µF/200V/
R2		C2	KMH/NCC
R4, R6, R8	3k 1/2W	C3	100nF
		C4	
R5	26k	C5	1µF
R7, R9	Pot 5k	C6	1nF
R10	270	C7	47nF
R11	1.8k	C8	8.2nF
R12, R13	10	C9	270pF
R14	0.3 (3X1Ω)	C10	100µF
R15	680	C11, C12	1.2nF
R16	30k	C13, C14	1.2nF
R17	4.7k	C15	560µF/25V/
R19		C16	LXF/NCC
R20	1k	C17, C18	1500µF/10V
		C19	LXF/NCC
R22	300	C25	100nF/63V
R23	510	C26	4.7nF/630V
R25	1.1k	C27	2.2nF 2kV
R26, R27	15 1W	C28	4.7nF
R28, R29	15 1W	C29	100nF
R30, R31	10k		
R35	1.1k	IC1	L4990
R36	2k	IC2	L6380
		IC3	TCDT1101GB
		IC4	TL431
		IC5	L4955

<b>Bridge Diode</b>	FBU 4M FAGOR
Q1	STP5NA60
Q2, Q3	STK2N60
Q4	BC337
D1, D2	STBYW99150
D3, D4	STPS3045CP
D5	1N4148
D6	GI UF 4007 (ultra fast)/600V
D7	22V Zener
D8	1N4148
L4	77930 5V (9T-18Wire - AWG26) 12V (12T-1Wire-AWG18)
T1	ETD39 3F3
<b>Primary:</b> 34T-1 Litz wire (0.1mm-60 wire) <b>Secondary 5V:</b> 3T-4 Litz wire (0.1mm-90 wire) <b>Secondary 12V:</b> 4T-1 Litz wire (0.1mm-60 wire) <b>Autosupply:</b> 7T	

**APPLICATION NOTE**

**Figure 10:** Components Layout.



**Figure 11a:** Printed circuit board. (Back side).

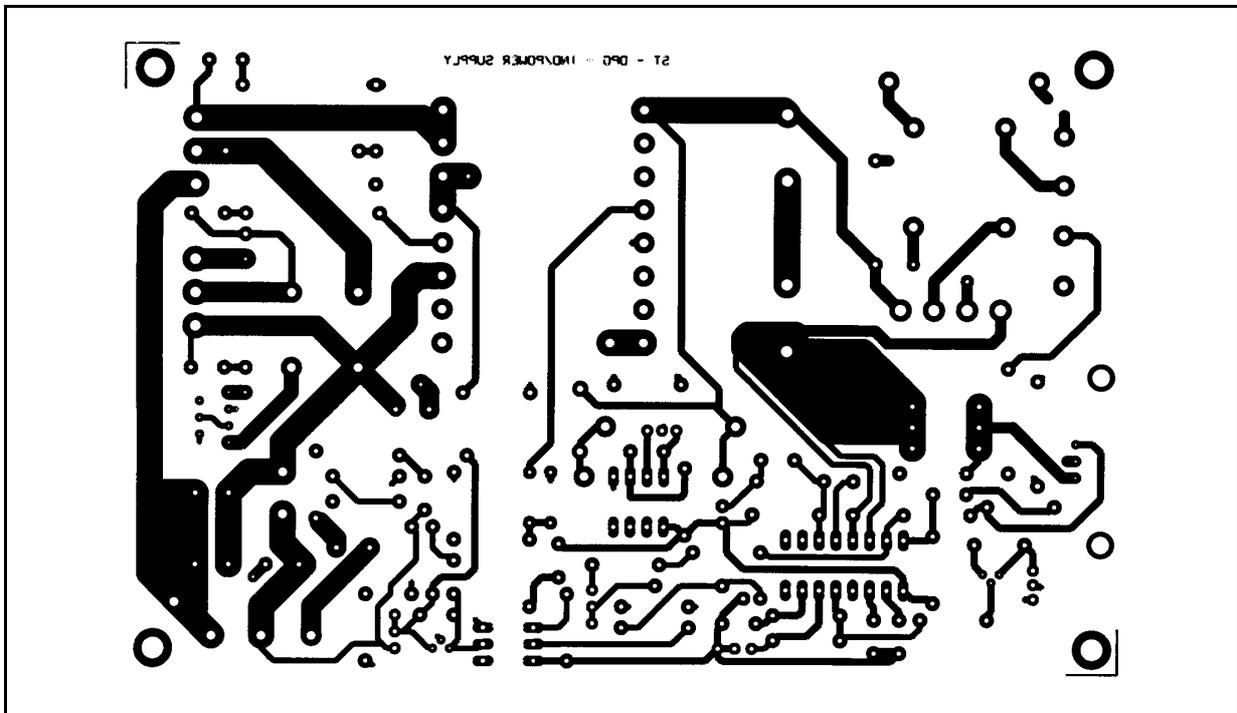
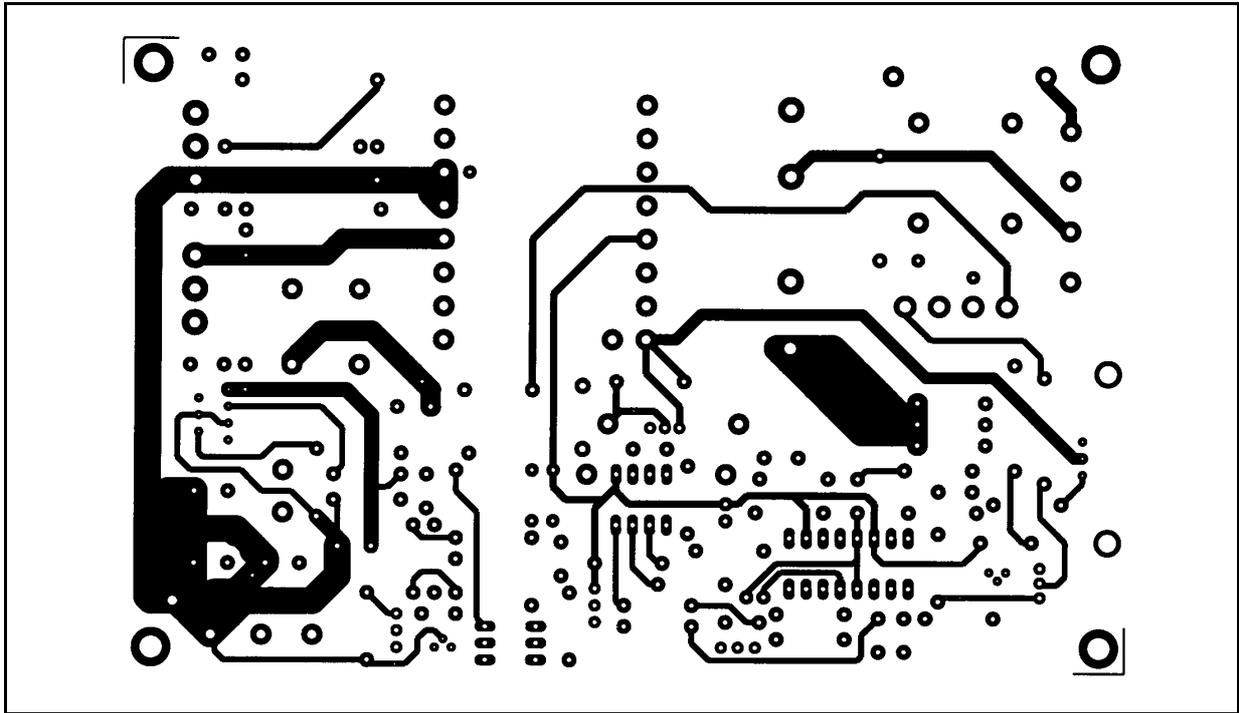


Figure 11b: Printed circuit board. (Component side).



**REFERENCES:**

[1] Efficient active Clamp for Off-line Applications using L4990 and L6380 (Tricomi N. - Gattavari G. - Adragna PCIM96 - NURBERG).

## APPLICATION NOTE

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