
TECHNICAL MANUAL

COMPACT DISC PLAYER

DOOMENKE

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1. FUNDAMENTALS

1-1 FUNDAMENTALS

1-1-1 Sampling

An analog voltage is continuous in respect to time, and has a value at each time of t_1, t_2, t_3 , etc. as shown in Fig. 1.1 and as well a value at any time between t_1 and t_2 .

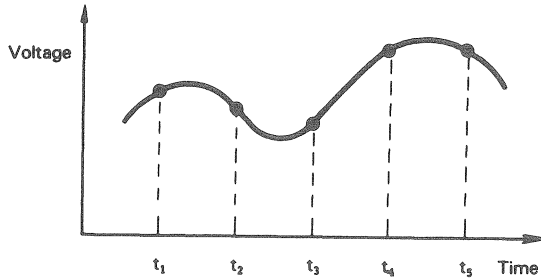


Fig. 1.1

If an analog voltage is represented corresponding to a code system, the analog voltage over the definite time range of t_1 to t_2 is made of the indefinite number of codes. In order to transmit a digital signal corresponding to the voltage at t_1 , it needs a definite time length, but when transmitting indefinite codes, the transmission does not end forever.

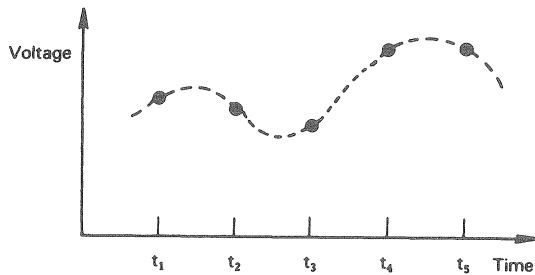


Fig. 1.2

Therefore, in case where an analog voltage is converted to a coded system, analog voltages at timings with some interval are only converted as shown in Fig. 1.2. With such a process, the definite number of codes corresponding to the definite timings, for example, five codes for the time interval t_1 to t_5 are produced.

When having transmitted codes described in Fig. 1.2, only five codes can be received at the receive side between t_1 and t_5 . The number of voltage values reproduced thereby is only five, any voltage at timings except t_1, t_2, t_3 , etc. cannot be determined.

However, if the frequency component (20 kHz) of the original analog signal is less than the value (44.1 kHz) depending upon the time interval between timings t_1, t_2, t_3 , etc. at which coding is staged, even the value for non-transmitted portions can be reproduced. To pick up analog values at a fixed time interval by such a process is called "sampling".

1-1-2 Quantization

Fig. 1.3 indicates one example where analog signals ranging from 0V to 10V are converted to 11-step voltage values of 0V, 1V, 2V,...,9V and 10V via round-off. With this conversion, preparation of only 11 kinds of codes is needed. To convert an analog signal to a kind of a digital signal with the process of round-off or the like is called "Quantization".

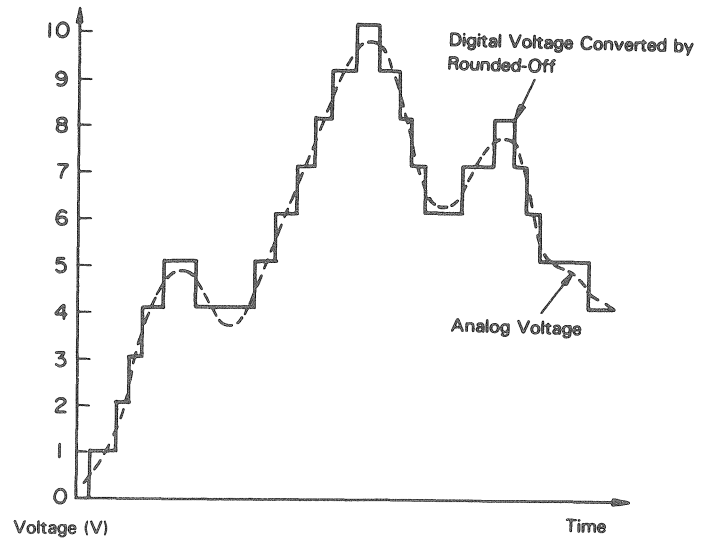
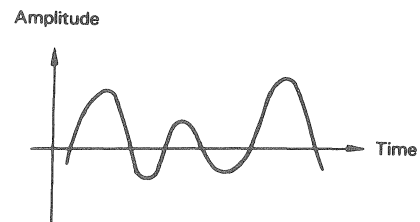
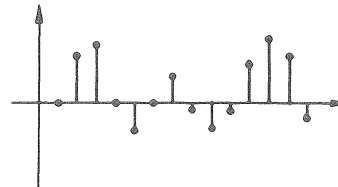


Fig. 1.3



↓ Sampling



↓ Quantization

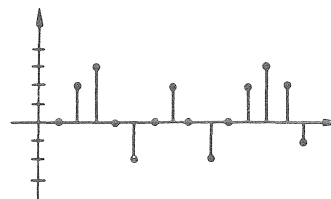


Fig. 1.4

1. FUNDAMENTALS

1-1-3 Sampling theorem

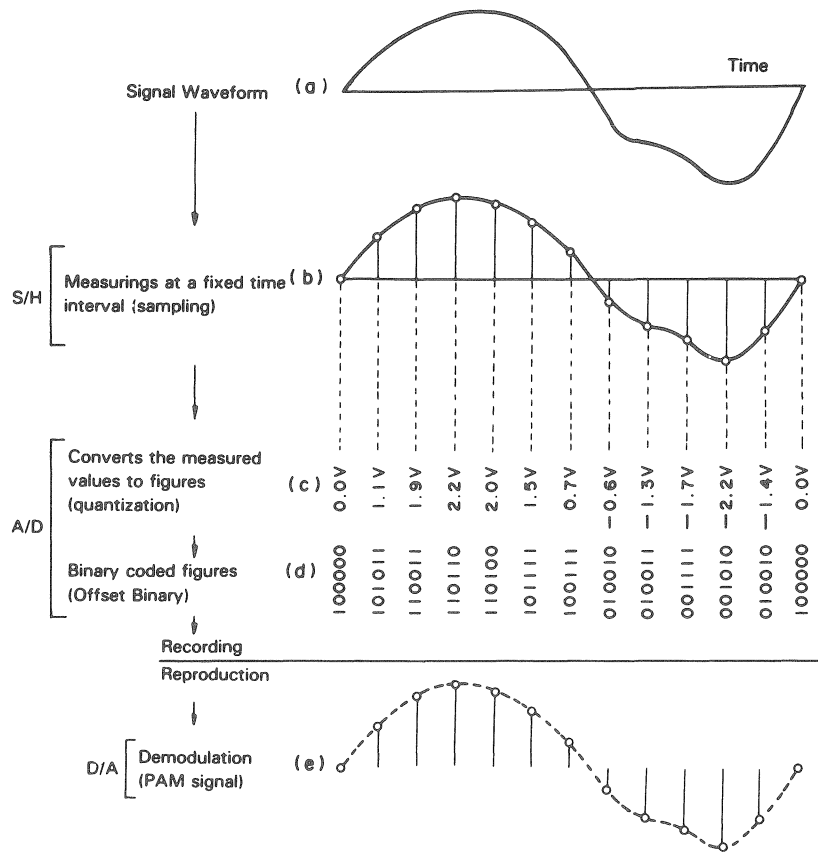


Fig. 1.5

The frequency of picking up an analog signal, for example, 50,000 times per second, is called "a sampling frequency. It is proven that if sampling is conducted at the rate larger than a certain value, the original waveform can be reproduced just the same to an inch. This is called "a sampling theorem".

Sampling Theorem: If sampling is conducted at the frequency (44.1 kHz) which is over double the maximum frequency (20 kHz) in a spectrum of a signal, the original waveform can be completely reproduced.

1. FUNDAMENTALS

1-1-4 Quantizing noises

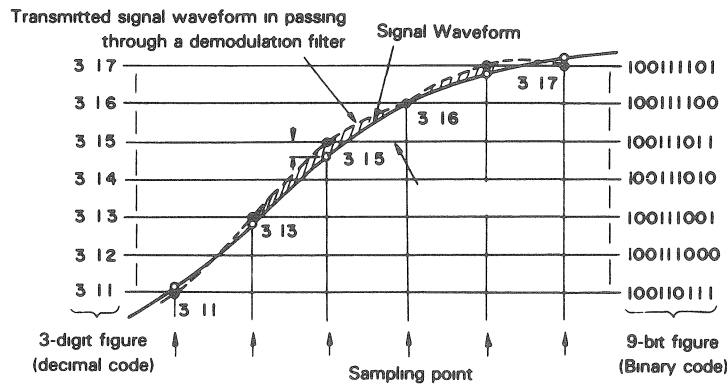


Fig. 1.6

A rounding error is caused by quantization at sampling points as described in 1-2, and seeing Fig 1 6 it can be thought that this rounding error is created as a distortion or noise. This

noise is of the nature different from noises emitted from an analog system, being called "a quantization noise".

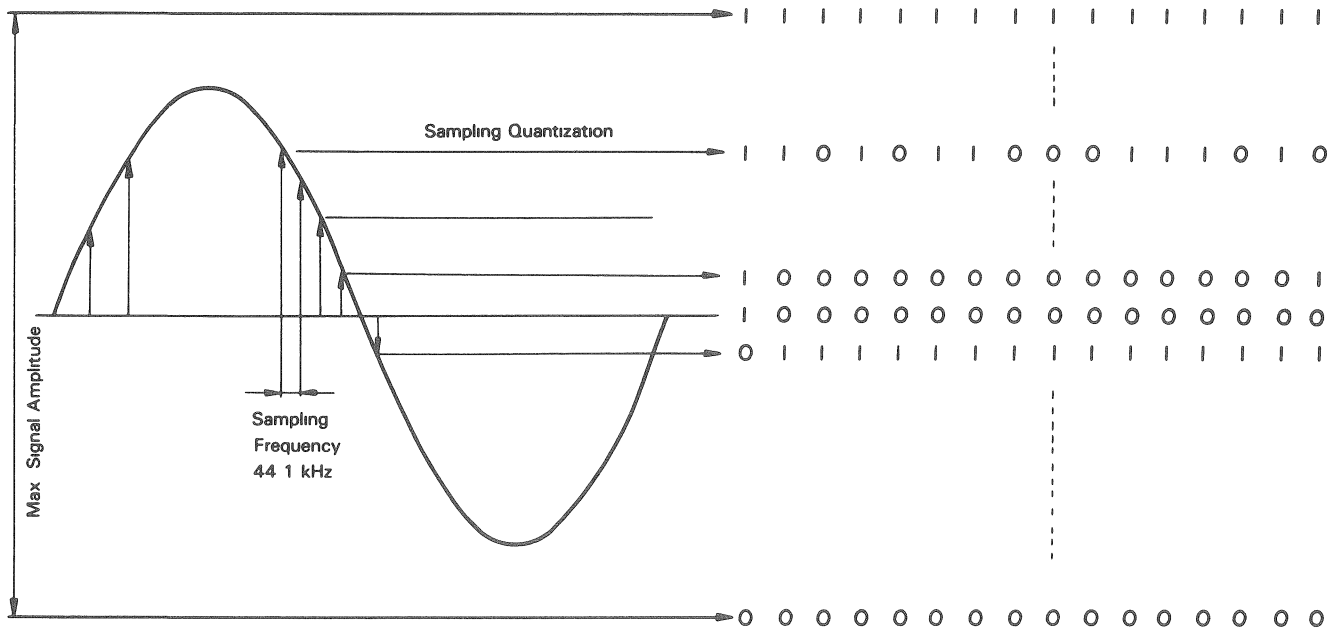


Fig. 1.7

The ratio of a quantizing noise against the maximum value of the signal in a binary-coded 16-bit system is plotted in respect to a sinusoidal wave input as shown in Fig 1 7

If a 16-bit code is used in quantizing one sampled value, the number of steps which can be taken, i.e., the quantizing number N is given as follows

$$N = 2^{16} = 65536$$

When making the amplitude of 0 to V corresponding to this, the width E_0 of one quantization step is given by

$$E_0 = V / (N - 1)$$

Therefore, the amplitude of a quantizing noise is E_0 at the peak-to-peak value, so that the noise power N_Q is

$$N_Q = \frac{2}{E_0} \int_0^{E_0} X^2 dX = \frac{E_0^2}{12}$$

1. FUNDAMENTALS

On the other hand, supposing that an input signal is a sinusoidal wave whose amplitude at the peak-to-peak value is V , the signal power S is:

$$S = \frac{1}{2\pi} \int_0^{2\pi} \left(\frac{V}{2} \sin X \right)^2 dX = \frac{V^2}{8}$$

Therefore, the power ratio is:

(Dynamic range of the Compact Disc system is)

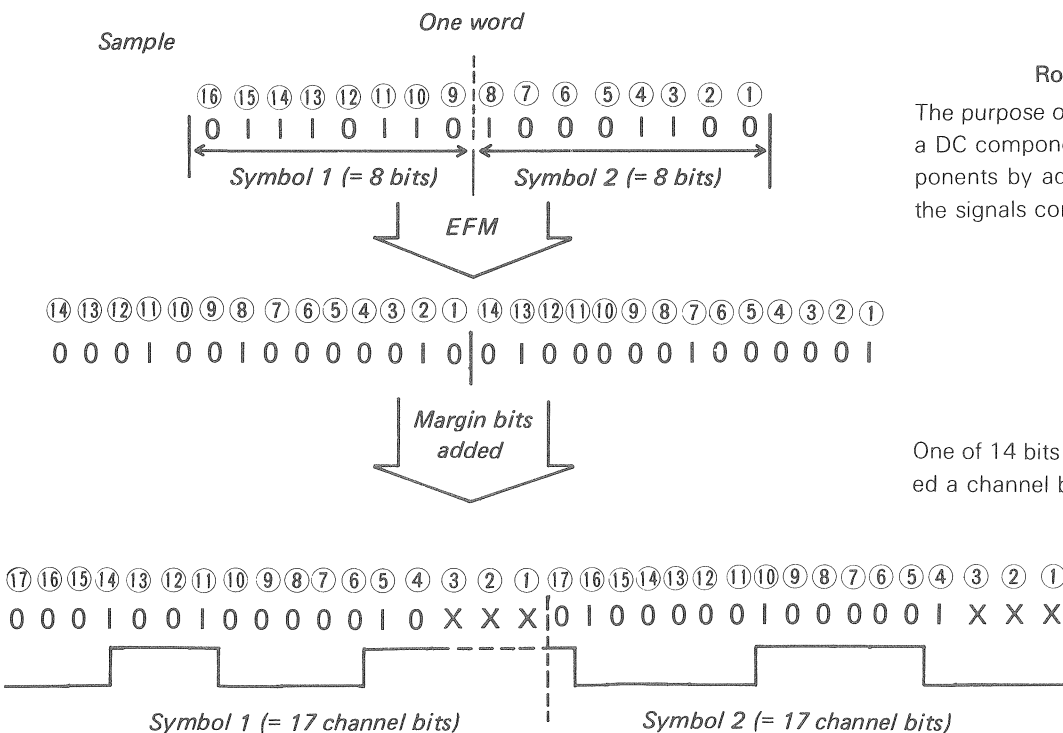
$$\frac{S}{N_q} = \frac{V^2}{8} / \frac{E_o^2}{12} = \frac{3}{2} (N-1)^2$$

$$D = 10 \log \frac{S}{N_q} = 10 \log \frac{3}{2} (2^{16} - 1)^2 \div 98 \text{ dB}$$

1-1-5 EFM (Eight to Fourteen Modulation)

To convert a level of an analog signal at every interval of a fixed period ($1/44.1 \text{ kHz} = 22.7 \mu\text{s}$), as described in 1-1-4, to a binary code (1 and 0) after quantization is called a "PCM" (Pulse Code Modulation).

PCM has various kinds of modulation systems, but here a Sony and Philips jointly developed new system, called EFM, used for DAD is described.



Role of Margin Bits

The purpose of the margin bits is to reduce a DC component and low frequency components by adding three additional bits to the signals converted into EFM.

Channel Bits

One of 14 bits converted from 8 bits is called a channel bit.

Fig. 1.8

- (1) EFM is the modulation to first divide a 16-bit datum (data bit) into two 8-bit data and then convert each of these 8-bit data to a 14-bit datum (channel bit) as shown in Fig. 1.8. The conversion is to select patterns of 2^8 kinds among patterns of 2^{14} kinds, meeting the following condition. Channel bits of 2^8 meeting this condition have been predetermined by a computer as indicated in Tables 1-1 and 1-2:

Two or more but 10 or less 0s (zeros) should be always inserted between channel bits 1.

- (2) Three channel bits are always inserted between 14-bit blocks. The role of these 3 bits is to make adjustment so that the above condition (enclosed in the box) is met even at the connection of blocks.

1. FUNDAMENTALS

Order	8 bits→14 bits	
	data bits	channel bits
0	00000000	01001000100000
1	00000001	10000100000000
2	00000010	10010000100000
3	00000011	10001000100000
4	00000100	01000100000000
5	00000101	00000100010000
6	00000110	00010000100000
7	00000111	00100100000000
8	00001000	01001001000000
9	00001001	10000001000000
10	00001010	10010001000000
11	00001011	10001001000000
12	00001100	01000001000000
13	00001101	00000001000000
14	00001110	00010001000000
15	00001111	00100001000000
16	00010000	10000000100000
17	00010001	10000010000000
18	00010010	10010010000000
19	00010011	00100000100000
20	00010100	01000010000000
21	00010101	00000010000000
22	00010110	00010010000000
23	00010111	00100010000000
24	00011000	01001000010000
25	00011001	10000000010000
26	00011010	10010000010000
27	00011011	10001000010000
28	00011100	01000000010000
29	00011101	00001000010000
30	00011110	00010000010000
31	00011111	00100000010000
32	00100000	00000000100000
33	00100001	10000100001000
34	00100010	00001000100000
35	00100011	00100100100000
36	00100100	01000100001000
37	00100101	00000100001000
38	00100110	01000000100000
39	00100111	00100100001000
40	00101000	01001001001000
41	00101001	10000001001000
42	00101010	10010001001000
43	00101011	10001001001000
44	00101100	01000001001000
45	00101101	00000001001000
46	00101110	00010001001000
47	00101111	00100001001000
48	00110000	00000100000000
49	00110001	100000100001000
50	00110010	100100100001000
51	00110011	10000100010000
52	00110100	010000100001000
53	00110101	000000100001000
54	00110110	000100100001000
55	00110111	0010000100001000
56	00111000	01001000001000
57	00111001	10000000001000
58	00111010	10010000001000
59	00111011	10001000001000
60	00111100	01000000001000
61	00111101	00001000001000
62	00111110	00010000001000
63	00111111	00100000001000

↓ ↓ ↓ ↓
 d1d8 C1.....C14
 C1 is first cut.

Order	8 bits→14 bits	
	data bits	channel bits
64	01000000	01001000100100
65	01000001	10000100100100
66	01000010	10010000100100
67	01000011	10001000100100
68	01000100	01000100100100
69	01000101	00000000100100
70	01000110	00010000100100
71	01000111	00100100100100
72	01001000	01001001000100
73	01001001	10000001000100
74	01001010	10010001000100
75	01001011	10001001000100
76	01001100	01000001000100
77	01001101	00000001000100
78	01001110	00010001000100
79	01001111	00100001000100
80	01010000	10000000100100
81	01010001	10000010000100
82	01010010	10010010000100
83	01010011	00100000100100
84	01010100	01000010000100
85	01010101	00000010000100
86	01010110	00010010000100
87	01010111	00100010000100
88	01011000	01001000000100
89	01011001	10000000000100
90	01011010	10010000000100
91	01011011	10001000000100
92	01011100	01000000000100
93	01011101	00001000000100
94	01011110	00010000000100
95	01011111	00100000000100
96	01100000	01001000100010
97	01100001	10000100100010
98	01100010	10010000100010
99	01100011	10001000100010
100	01100100	01000100100010
101	01100101	00000000100010
102	01100110	01000000100010
103	01100111	00100100100010
104	01101000	01001001000010
105	01101001	10000001000010
106	01101010	10010001000010
107	01101011	10001001000010
108	01101100	01000001000010
109	01101101	00000001000010
110	01101110	00010001000010
111	01101111	00100001000010
112	01110000	10000000100010
113	01110001	10000010000010
114	01110010	10010010000010
115	01110011	00100000100010
116	01110100	01000010000010
117	01110101	00000010000010
118	01110110	00010010000010
119	01110111	00100010000010
120	01111000	01001000000010
121	01111001	00001001001000
122	01111010	10010000000010
123	01111011	10001000000010
124	01111100	01000000000010
125	01111101	00001000000010
126	01111110	00010000000010
127	01111111	00100000000010

EFM Conversion table 0 to 127
(NRZ-I representation)

1. FUNDAMENTALS

Order	8 bits→14 bits	
	data bits	channel bits
128	10000000	01001000100001
129	10000001	10000100100001
130	10000010	10010000100001
131	10000011	10001000100001
132	10000100	01000100100001
133	10000101	00000000100001
134	10000110	00010000100001
135	10000111	00100100100001
136	10001000	01001001000001
137	10001001	100000001000001
138	10001010	10010001000001
139	10001011	10001001000001
140	10001100	01000001000001
141	10001101	00000001000001
142	10001110	00010001000001
143	10001111	00100001000001
144	10010000	10000000100001
145	10010001	10000010000001
146	10010010	10010010000001
147	10010011	00100000100001
148	10010100	01000010000001
149	10010101	00000010000001
150	10010110	00010010000001
151	10010111	00100010000001
152	10011000	01001000000001
153	10011001	10000010010000
154	10011010	10010000000001
155	10011011	10001000000001
156	10011100	01000010010000
157	10011101	00001000000001
158	10011110	00010000000001
159	10011111	00100010010000
160	10100000	00001000100001
161	10100001	10000100001001
162	10100010	01000100010000
163	10100011	00000100100001
164	10100100	01000100001001
165	10100101	00000100001001
166	10100110	01000000100001
167	10100111	00100100001001
168	10101000	01001001001001
169	10101001	10000001001001
170	10101010	10010001001001
171	10101011	10001001001001
172	10101100	01000001001001
173	10101101	00000001001001
174	10101110	00010001001001
175	10101111	00100001001001
176	10110000	00000100100000
177	10110001	10000010001001
178	10110010	10010010001001
179	10110011	00100100010000
180	10110100	01000010001001
181	10110101	00000010001001
182	10110110	00010010001001
183	10110111	00100010001001
184	10111000	01001000001001
185	10111001	10000000001001
186	10111010	10010000001001
187	10111011	10001000001001
188	10111100	01000000001001
189	10111101	00001000001001
190	10111110	00010000001001
191	10111111	00100000001001

d1d8

C1.....C14

C1 is first cut.

Order	8 bits→14 bits	
	data bits	channel bits
192	11000000	01000100100000
193	11000001	10000100010001
194	11000010	10010010010000
195	11000011	00001000100100
196	11000100	01000100010001
197	11000101	00000100010001
198	11000110	00010010010000
199	11000111	00100100010001
200	11001000	00001001000001
201	11001001	10000100000001
202	11001010	000010010000100
203	11001011	00001001000000
204	11001100	01000100000001
205	11001101	00000100000001
206	11001110	00000010010000
207	11001111	00100100000001
208	11010000	00000100100100
209	11010001	10000010010001
210	11010010	10010010010001
211	11010011	10000100100000
212	11010100	01000010010001
213	11010101	00000010010001
214	11010110	00010010010001
215	11010111	00100010010001
216	11011000	01001000010001
217	11011001	1000000010001
218	11011010	10010000010001
219	11011011	10001000010001
220	11011100	01000000010001
221	11011101	00001000010001
222	11011110	00010000010001
223	11011111	00100000010001
224	11100000	01000100000010
225	11100001	00000100000010
226	11100010	10000100010010
227	11100011	00100100000010
228	11100100	01000100010010
229	11100101	00000100010010
230	11100110	01000000100010
231	11100111	00100100010010
232	11101000	10000100000010
233	11101001	10000100000100
234	11101010	00001001001001
235	11101011	00001001000010
236	11101100	01000100000100
237	11101101	00000100000100
238	11101110	00010000100010
239	11101111	00100100000100
240	11110000	00000100100010
241	11110001	10000010010010
242	11110010	10010010010010
243	11110011	00001000100010
244	11110100	01000010010010
245	11110101	00000010010010
246	11110110	00010010010010
247	11110111	00100010010010
248	11111000	01001000010010
249	11111001	10000000010010
250	11111010	10010000010010
251	11111011	10001000010010
252	11111100	01000000010010
253	11111101	00001000010010
254	11111110	00010000010010
255	11111111	00100000010010

data bits

channel bits

EFM Conversion table 128 to 255
(NRZ-I presentation)

cf: NRZ Non Return to Zero

1. FUNDAMENTALS

1-1-6 Frame synchronization and frame structure

Reproduction signals cannot be recovered if RF signals do not come out for a long time due to dropout or one information bit has been shifted owing to jittering in digital recording or playback. Because one bit shift of a digital signal makes the signal quite different in its signal level.

Therefore, by dividing a recorded signal to many small blocks, the system is organized so that even when a signal is disturbed due to jittering or the like, a bit synchronization is always established at the new block to identify the joint part between blocks. Such a block is called a "Frame". Frame Sync signals are inserted to indicate the boundary of the frame and to make a bit synchronization. Fig. 1.9 shows the structure of one frame.

	Channel bits	Margin bits	Total bits
Frame Synchronization	24	3	27
Users bits	14	3	17
Data bits	$14 \text{ bit} \times 24 = 336$	$3 \text{ bit} \times 24 = 72$	408
Error correction bits (Parity bits)	$14 \text{ bit} \times 8 = 112$	$3 \text{ bit} \times 8 = 24$	136
	486	102	588

Frame Structure

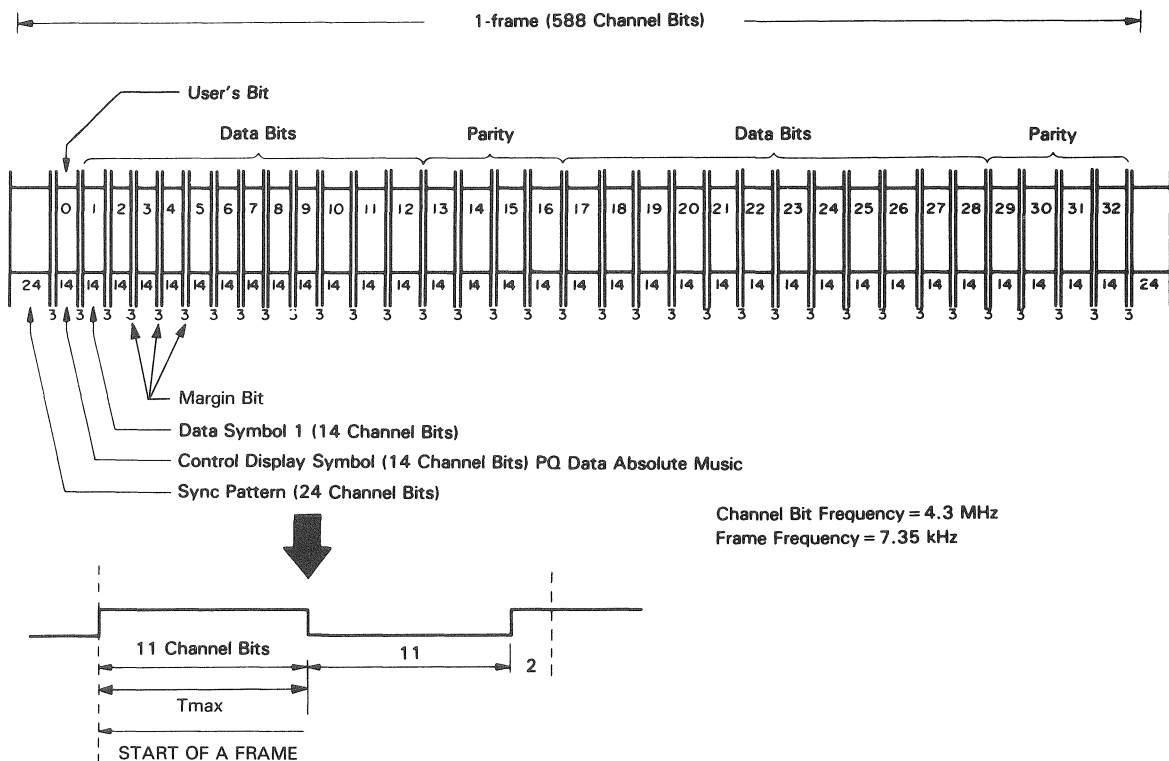


Fig. 1.9

1. FUNDAMENTALS

1-2 USER'S BIT

1-2-1 Address Data (Q Signal)

1) Address Data (Q Signal) Reading Section

In the CD system specifications, one symbol consisting of 8 bits and located after frame synchronization signal of PCM data is called CONTROL & DISPLAY SYMBOL, and each of 8 bits is called P-Channel, Q-Channel,

R-Channel....& W-Channel. Of the eight channels, Q-Channel is used for address data and one address data is comprized of 98 frame Q-Channel data. Fig. 1-10 shows this configuration of the CONTROL & DISPLAY symbol data.

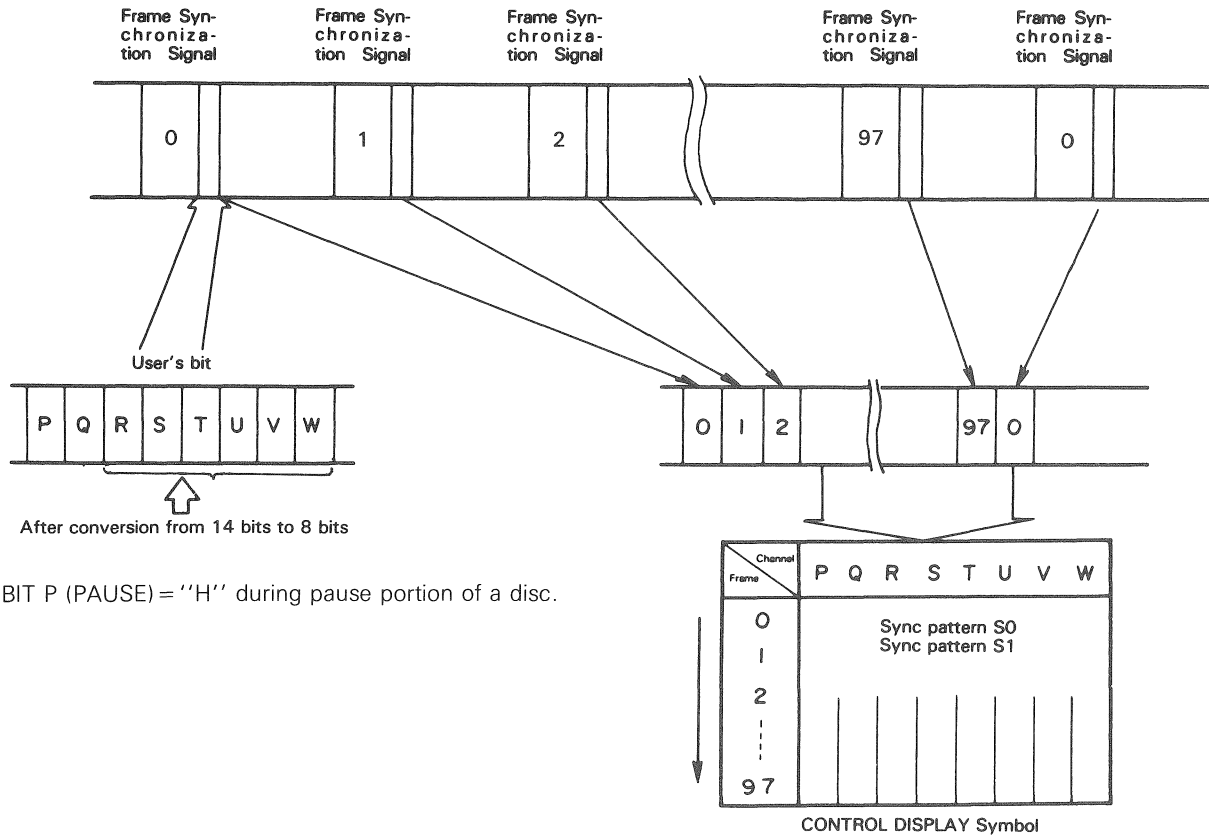


Fig. 1-10

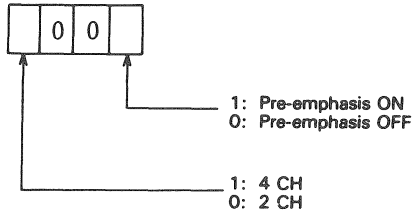
- 2) Those BIT R,S,...W are used to display. For example, still picture on a TV set.

1. FUNDAMENTALS

Address data format (outside lead-in area) are as follows:

S0, S1: 2 bits address signal sync pattern.

CONTROL: 4 bits control data, MSB indicates pre-emphasis on or off, and LSB indicates 4CH/2CH.



ADR: 4 bit mode data

MODE 1 (1 in BCD): Address mode

MODE 2 (2 in BCD): Disc catalog number mode

MODE 3 (3 in BCD): Special information mode (recorded by alphanumeric code 0-9, A-Z)

MNR: Program number expressed by BCD in 2 digits (8 bits)

X: Index for each program expressed by BCD in 2 digits (8 bits)

MIN: Elapsed time (minute) for each program expressed by BCD in 2 digits (8 bits)

FRAME: Elapsed time for each program expressed by BCD in 2 digits (8 bits) (Frame, 1 frame = 1/75 sec)

ZERO: Not used (8 bits zero data)

A MIN: Elapsed time (sec) for disc expressed by BCD in 2 digits (8 bits)

A SEC: Elapsed time (sec) for a disc expressed by BCD in 2 digits (8 bits)

A FRAME: Elapsed time for a disc expressed by BCD in 2 digits (8 bits) (frame).

CRC: 16 bit CRC code data calculated for data control of a frame.

Fig. 1-11 Shows the address data configuration.

Each figure under a code shows number of bits required for the code.

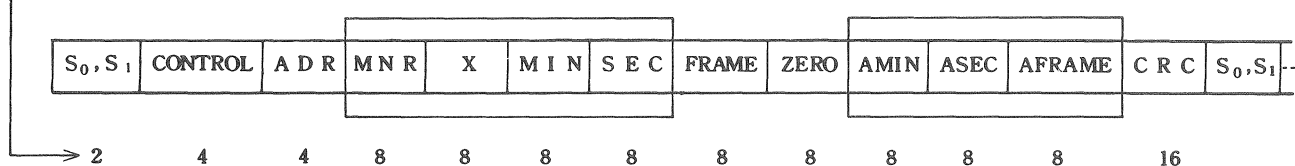


Fig. 1-11 Address Data configuration

THOSE CODE MNR:, X:, and MIN: are used to display the current playback position on the CD player.

1. FUNDAMENTALS

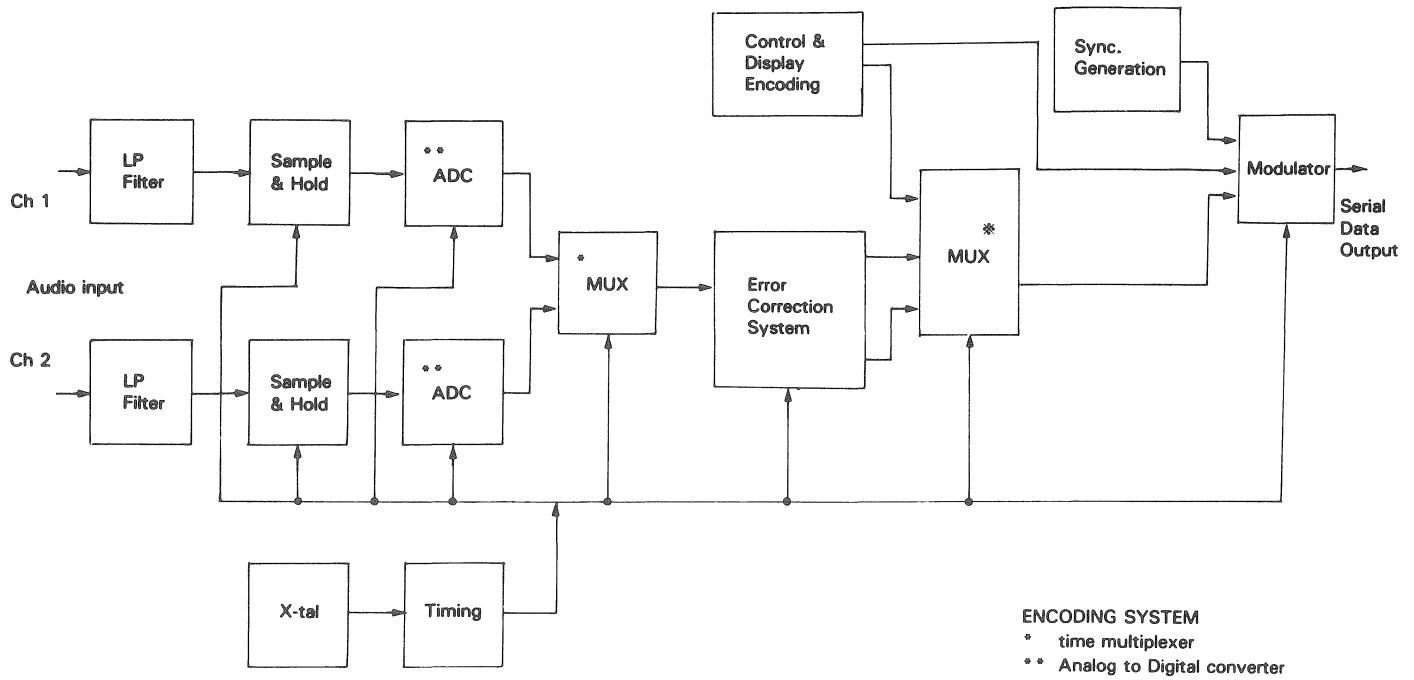


Fig. 1-12 Encoding system

1. FUNDAMENTALS

1-3 CODE ERROR

1-3-1 Causes of code error

- (1) Defectives which are already present on a disc at delivery
 - Dusts attached to pits during production of disc
 - Disc molding distortion (entering of air bubbles whose refraction factor is not equal)
- (2) Faults created on handling of a disc dusts, scratches, stains and finger prints
- (3) Level variations of reproduction signal (eye pattern)
Because protection of out-of-tracking, Focus and CLV are all depending on a servo system, poor stability of the servo leads to increased code errors

1-3-2 Kinds of code error

- (1) Random Error an error which causes an error in one bit
- (2) Burst Error an error which causes an error in many successive bits

1-3-3 Interleave

Even if reading every page of a book slantwise from its upper left side to lower right side, you can fully recognize the context or contents. However, you cannot recognize the contents of the book if you are reading carefully one character or clause without reading several tens of pages.

An error correction code is the same as this, and correction is easy even when code errors of some bits are present. However, if many, say 1000, bits are consecutively wrong at a time, it is very difficult to correct those errors.

Therefore, the technique with which an order of a signal is once changed and then recorded and, after reproduction, returned back to the original order is employed. This changing of the order of a signal is called an "interleave", and the returning to the original order is called a "deinterleave".

Fig. 1-13 is the illustration explaining the principle of interleave. The order of a signal at fabrication of the disc is out of order. Therefore, by deinterleaving the signal, successive code errors are dispersed, so that operation of error correction and associated jobs are made facilitative.

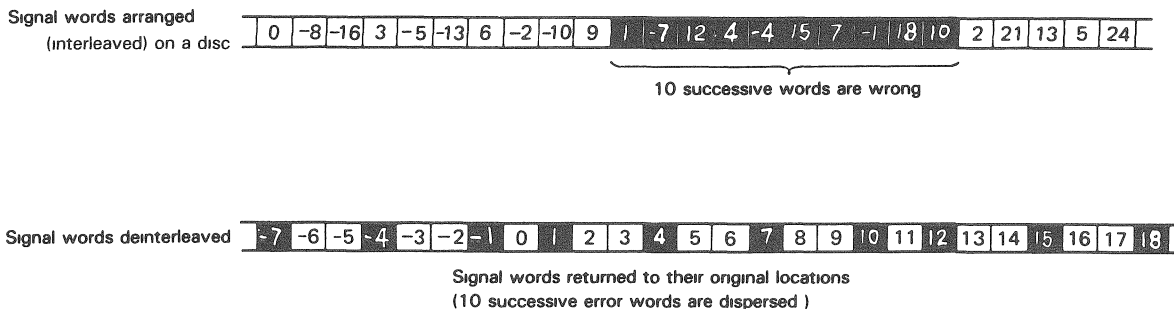


Fig. 1-13

1. FUNDAMENTALS

1-3-4 Single erasure correcting method

- (1) Bill (a) as shown in Fig. 1-14 indicates prices of four kinds of articles A, B, C and D and the total. In bill (b), the price of article B disappears. This calls a disappearance or erasure. When the total amount is known, the price of article B can be found even if one figure is missed. In the coding theory, whether the total amount is correct in bill (a) is checked. This operation is called "syndrome".

Bill (a)			
	A ¥	100	
	B ¥	200	
	C ¥	300	
+	D ¥	400	
Total P ¥			1,000

Syndrome (Checking)

$$S = A + B + C + D - P = 0$$

- (2) In bill (b), the price of article B disappears. (It is indicated by B^* . $B^* = 0$) Conducting the syndrome does not create $S = 0$ because there is an erasure. However, as the number of erasure is one, the amount of B^* can be found from syndrome $S = -200$. According to the single diserasure correcting method, operation of correction is conducted on the assumption that all other data (A' , C' and D') are correct. If there is an error for another article, miscorrection happens.

Bill (b)			
	A' ¥	100	
	B* ¥	?	
	C' ¥	300	
+	D' ¥	400	
Total P' ¥			1,000

← Disappearance

Syndrome (Checking)

$$S = A' + B' + C' + D' - P = 0$$

$$B = B^* - S = 200$$

- (3) Operating the syndrome on bill (c), zero does not come out. Therefore, it may be found that something is wrong, but it cannot be found which of A' , B' , C' , D' and P' is incorrect. In such a case, correction is infeasible.

Bill (c)			
	A' ¥	100	
	B' ¥	300	
	C' ¥	300	
+	D' ¥	400	
Total P' ¥			1,000

$$S = A' + B' + C' + D' - P' = 0$$

- (4) Bill (d) illustrates the example that the location to be corrected is known, and the correction can be done by the same means as in bill (b). The means to indicate the location of error in such a way is called a "pointer".

In the examples of (1) to (4), "Total P'" is used for check of error or erasure of data A, B, C and D. A word used for check and correction besides required data is called a "parity word" or a "parity bit".

Bill (d)			
	A' ¥	100	
	B* ¥	300	
	C' ¥	300	
+	D' ¥	400	
Total P' ¥			1,000

$$S = A' + B' + C' + D' - P' = 100$$

$$B = B^* - S = 200$$

Fig. 1-14

1. FUNDAMENTALS

1-3-5 Single error correction, double erasures

- (1) In case of (3) in 3-4, correction is infeasible because the location of error is unknown. Even in such a case, the way by which correction is feasible is a single error correcting method. In 3-4, there is only one parity word, P. Besides this, a "Weighted Total Value", Q, is used. Because two parity words P and Q are used, there are also two syndromes S_1 And S_2 .

Now suppose that there is an incorrect bill (b) in respect to a correct bill (a) and that the location of error (one) in bill (b) is unknown.

Supposing that the differences from original values are E_A, E_B, E_C, E_D, E_P and E_Q with respect to A', B', C', D', P' and Q' , respectively, of bill (b) (for no error, E_A to $E_Q = 0$)
 $A' = A + E_A, B' = B + E_B, C' = C + E_C, D' = D + E_D,$
 $P' = P + E_P, Q' = Q + E_Q$

Obtaining syndrome S_1 ,

$$\begin{aligned} S_1 &= A' + B' + C' + D' - P' \\ &= (A + E_A) + (B + E_B) + (C + E_C) + (D + E_D) - (P + E_P) \\ &= \underbrace{A + B + C + D - P}_0 + E_A + E_B + E_C + E_D - E_P - (1) \\ &= E_A + E_B + E_C + E_D - E_P \end{aligned}$$

Obtaining syndrome S_2

$$\begin{aligned} S_2 &= 4A' + 3B' + 2C' + D' - Q' \\ &= \underbrace{4A + 3B + 2C + D - Q}_0 + (4E_A + 3E_B + 2E_C + E_D - E_Q) \quad (2) \\ &= 4E_A + 3E_B + 2E_C + E_D - E_Q \end{aligned}$$

Supposing that a code error is one word between A' to P', Q'

- | | |
|------------------|-------------------------|
| (I) A' wrong | $S_1 = E_A, S_2 = 4E_A$ |
| (II) B' wrong | $S_1 = E_B, S_2 = 3E_B$ |
| (III) C' wrong | $S_1 = E_C, S_2 = 2E_C$ |
| (IV) D' wrong | $S_1 = E_D, S_2 = E_D$ |
| (VI) P' wrong | $S_1 = E_P, S_2 = 0$ |
| (VII) Q' wrong | $S_1 = 0, S_2 = -E_Q$ |

By a method where two syndromes are introduced as mentioned above and determined, wrong words can be found and corrected.

Bill (a)		
A	¥	100
B	¥	200
C	¥	300
D	¥	400
P	¥	1,000
Q	¥	1,000
P = A + B + C + D		
Q = 4A + 3B + 2C + D		

Syndromes

$$\begin{aligned} S_1 &= A + B + C + D - P = 0 \\ S_2 &= 4A + 3B + 2C + D - Q = 0 \end{aligned}$$

Bill (b)		
A'	¥	100
B'	¥	300
C'	¥	300
D'	¥	400
P'	¥	1,000
Q'	¥	2,000

Syndrome

$$\begin{aligned} S_1 &= A' + B' + C' + D' - P' = 100 \\ S_2 &= 4A' + 3B' + 2C' + D' - Q' = 300 \end{aligned}$$

Fig. 1-15

1. FUNDAMENTALS

- (2) The principle of double erasure correction is described below. In this case, the location of error is indicated with a pointer. It is here known that two words in bill (c) are wrong and there are no other wrong words. Using equation (1) in paragraph (1),

$$S_1 = \underbrace{A + B + C + D - P}_{=0} + E_A + E_B + E_C + E_D - E_P = 200$$

Supposing $E_A = 0$, $E_D = 0$ and $E_P = 0$

$$S_1 = E_B + E_C = 200 \quad (3)$$

From Equation (2) of (1)

$$S_2 = \underbrace{4A + 3B + 2C + D}_{=0} + (4E_A + 3E_B + 2E_C + E_D - E_Q) = 500$$

$$S_2 = 3E_B + 2E_C = 500 \quad (4)$$

Determining E_B and E_C from simultaneous equations of (3) and (4),

Bill (c)		
A' ¥	100	
B' ¥	300	← Pointer
C' ¥	400	
D' ¥	400	
P' ¥	1,000	
Q' ¥	2,000	

$$E_B = 100$$

$$E_C = 100$$

$$S_1 = A' + B^* + C^* + D' - P' = 200$$

$$S_2 = 4A' + 3B' + 2C^* + D' - Q' = 500$$

Where

$$B^* = E + E_B \quad C^* = C + E_C$$

Fig. 1-16

This theory is the principle of a Reed Solomon Code. In practice, the Reed Solomon Code with four parity words is used.

1. FUNDAMENTALS

1-3-6 Cross-interleave

- (1) Fig. 1-17 Shows a principle of a cross-interleave. An original series of signals is divided into a number of words, and parity words are inserted.

$$\begin{aligned} P_1 &= W_1 + W_2 + W_3 + W_4 \\ P_5 &= W_5 + W_6 + W_7 + W_8 \\ P_9 &= W_9 + W_{10} + W_{11} + W_{12} \end{aligned} \quad (5)$$

Four original series of signals ($W_1, W_5, W_9, W_{13}, \dots$) ($W_2, W_6, W_{10}, W_{14}, \dots$), ($W_3, W_7, W_{11}, W_{15}, \dots$) and ($W_4, W_8, W_{12}, W_{16}, \dots$) among many original series of signals are arranged for four lines No. 1 via No. 4 in Fig. 1-17 of these words, the words passing through No. 1 are

delivered directly, but words fed into No. 2 to No.4 lines are subject to delay with delay memories by one to three words so that the word order is changed (interleaved) at their respective terminals.

There is an adder following the delay memories, where another parity word Q is created.

$$\begin{aligned} Q_1 &= W_1 + W_2 + W_5 + W_8 + W_{15} \\ Q_5 &= W_5 + W_2 + W_{-1} + W_{-4} + P_{-11} \\ Q_9 &= W_9 + W_6 + W_3 + W_0 + P_{-7} \end{aligned} \quad (6)$$

In other words, two system of codes are used on both sides of the delay memories.

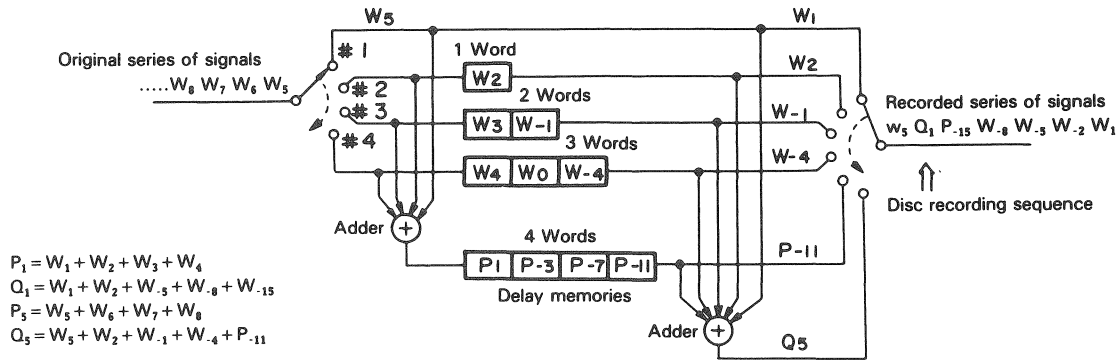


Fig. 1-17 Principle of Cross-Interleave Encoder

- (2) Fig. 1-18 indicates relations between two parity codes. The solid lines mean a P's series, and the dotted lines mean a Q's series. Each of them has the capability of single erasure correction, so that n error of a single word can be easily corrected of course.

The syndrome of each other's series can be used as a pointer for pointing out a location of error.

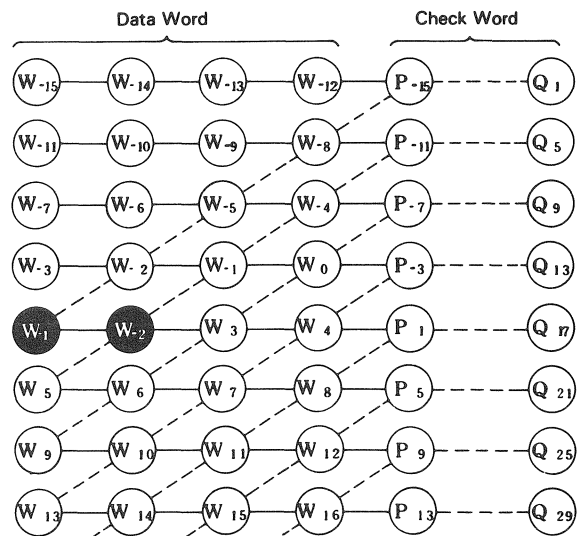
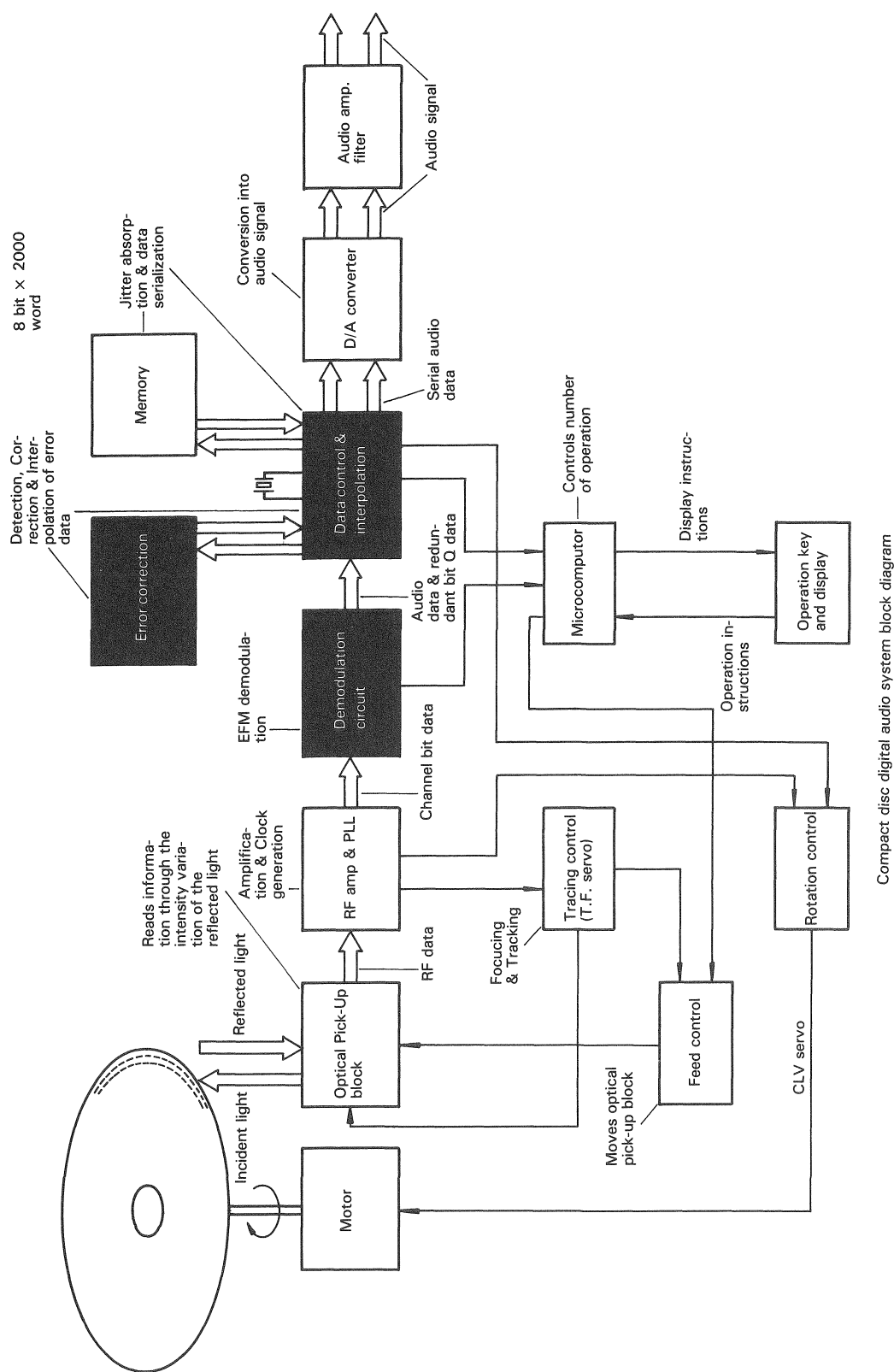


Fig. 1-18 Code Series of Cross Interleave
(Black shades indicate errors).

2. DESCRIPTION OF FUNDAMENTALS CIRCUIT



Compact disc digital audio system block diagram

Fig. 2-1

2. DESCRIPTION OF FUNDAMENTALS CIRCUIT

2-1. PRINCIPLE

The attached diagram is the block diagram of a CD player. The description in this manual will be given following the flow of signal.

2-1-1 Laser Pickup (Optical System)

The laser diode generates laser light and applies it to the disc surface through prisms and lenses. The light reflected from the disc surface, the degree of interference of which varies depending on the presence or absence of data pit, is input to the pickup (as incident light) and converted into electrical signal level.

The laser beam is normally focused to $1.5\text{ }\mu\text{m}$ on the disc surface. When the circular beam is deformed or split due to degradation of the laser diode, etc., the S/N of the signal output from the pickup also degrades (containing more errors) and, in the worst case, playing could become impossible. The pickup is designed so that it outputs correct signals (data, tracking and focus error signals) when the laser light axis is perpendicular to the disc surface. This is why the radial, tangential and height adjustments are critical for the CD player performance.

Types of pickup

There are two types of pickups used in CD players, single-beam pickup used with the DP-1100 and other models, and 3-beam pickup used with models including the DP-7S.

As the 3-beam pickup is provided with an exclusive beam for the detection of tracking error and with an independent tracking error signal output, its subsequent servo circuit can be simpler compared to that of a single-beam pickup.

Note:

The laser diode may degrade or be internally damaged even with an instantaneous (in terms of nanosec) reverse voltage (in terms of a few volts). Therefore, servicing should be performed in an environment protected against the generation of static electricity.

Eye pattern

Eye pattern is the rhomboid waveform displayed when the pickup output is observed on an oscilloscope. The reproduction system including the disc is stable when the rhombuses are stable. Assuming $1T = 1/4.32\text{ MHz}$, only nine types of lengths are assigned for pits on the disc, 3T, 4T, 5T, 6T, 7T, 8T, 9T, 10T and 11T. This means that all data on a CD are represented using these nine waveforms.

When the CD output waveform is observed using an oscilloscope, the 3T, 4T, 11T waveforms and their combinations are displayed on the screen from left to right. As these are arranged in 1T intervals, the display as a whole looks like an eye pattern.

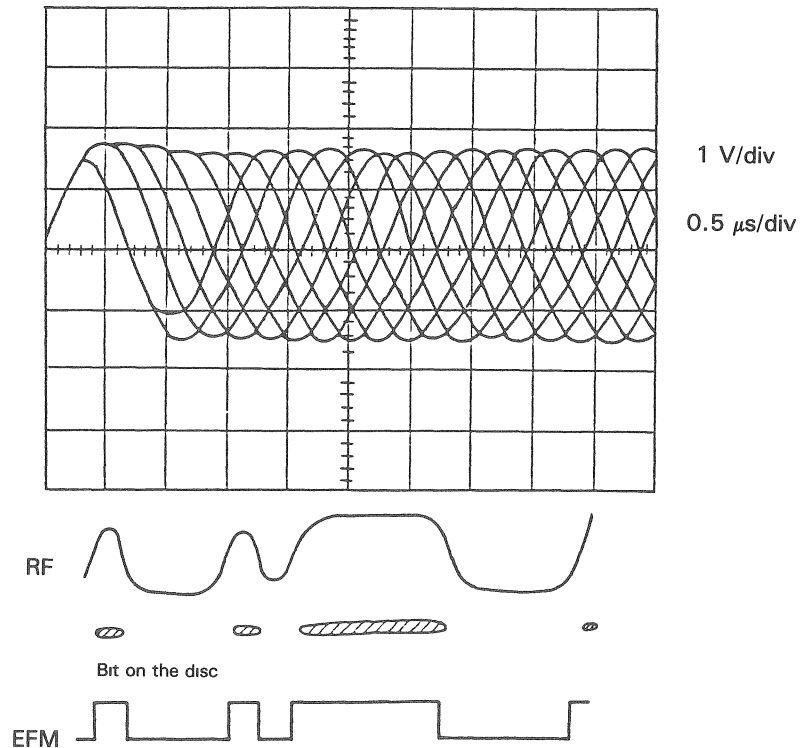


Fig. 2-2

2-1-2 RF Amplifier and PLL (Bit Synchronization)

As the pickup output level is as small as less than ten millivolts, it is amplified to a square wave by an RF amplifier before being converted into digital signals (EFM wave). The error signals are also generated in the RF amplifier and supplied to the focus and tracking servo circuitry.

Serial data are contained in the square wave obtained from the pickup output signal (data). To read the serial data correctly, a clock signal synchronized with the speed (frequency) of data signal is required.

The data rate is proportional to the disc rotation speed. It is zero at the moment the disc motor is started, attains the standard 4.32 Mbits/s (4.32 MHz) at a point and increases if the rotation speed is increased.

The clock (PLCK) which should vary in synchronism with such a varying signal is obtained using the PLL circuit. With the standard capturing range of $\pm 15\%$, the PLL tracks various frequency variations (wow & flutter) occurring in disc rotations to make possible the correct decoding of the EFM decoder in the following step.

The error signals for the tracking and focus servo circuitry are generated in the RF amplifier block and supplied to the servo circuitry. The signal generator circuitry varies depending on the pickup and circuit systems used, but the focus error signal is usually generated using the critical angle method (level difference detection) or astigmatism method, and the tracking error signal is usually generated using the phase difference method, 3-beam level difference method, push-pull method, etc.

2. DESCRIPTION OF FUNDAMENTALS CIRCUIT

2-1-3 EFM Decoder

Using the EFM signal and sync clock (PLCK) supplied from the RF amp, the EFM decoder block detects the frame sync signals which indicate the data sections. When a frame sync signal is detected, it converts thirty-three 14-bit symbol (data) into 8-bit data (EFM decoding) and store them in error correction memory.

The frame is repeated 7350 times a second. As each frame contains 588 bits of data, the data transfer speed is 4.32 MHz.

The frame sync signal is immediately followed by an 8-bit data called user's bits. Each of the 8 bits are assigned names P, Q, E, S, T, U, V and W.

By collecting 98 Q bits, information such as the time of points during playing can be obtained. When 6 bits from R to W are collected for one second, it is possible to acquire 44000 bits of data, which make it possible to display characters or still picture on a TV screen.

2-1-4 De-interleaving, Error Correction and Data Control

The output from the EFM decoder is stored in memory (max. 108/7350 second).

In this period, de-interleaving can be performed to re-arrange the order of data output which has been made discontinuous when recording the CD in order to facilitate error restoration, and data error can also be checked for performing error correction as required.

8 symbols among 32 data symbols in one frame holds the data used for inspection.

The speed of data output from the EFM decoder is higher when the motor rotation is faster and lower when it is slower. However, the speed of memory data readout and its output to the D/A converter is regulated at a constant speed by an X'tal oscillator control. In addition, the memory has a capacity of only 2000 symbols so it would overflow if too much data is output from the EFM decoder and would become empty in the opposite case.

This problem is solved by the CLV servo control. The description on the CLV servo is given in of section 2-1-7.

Data control block

The data control block controls the memory position where input data shall be stored, where the data to be supplied to the D/A converter is read from, and operations to respond to error correction requests.

The reason why wow & flutter is null:

Wow & flutter is contained in the memory input speed. However, the wow & flutter component of data is absorbed automatically when the data is stored in memory, because the speed of data output from memory to the D/A converter is X'tal controlled.

In consequence, this memory is called jitter-absorbing memory.

2. DESCRIPTION OF FUNDAMENTALS CIRCUIT

2-1-5 D/A Converter and Audio Block

After conversion from (8 x 2) to bit serial data, music signal data is supplied to the D/A converter together with sync signals.

The D/A converter uses the integrating type method for the digital-to-analog conversion. Digital data set to the counter inside the D/A converter is counted down at high speed. At the same time as the start of countdown, an external capacitor is charged by the constant current power supply. The charging is stopped when the counter attains zero, then the voltage across the two terminals of the capacitor is sampled to obtain

a voltage corresponding to the digital value. This conversion process contains no unstable factor in the short period used for conversion, offering very accurate conversion result.

The above operation is performed for each channel at a speed of 44.1 kHz.

Noise generated in the course of conversion is eliminated by supplying the converted signal to the circuit which extracts the stable voltage (deglitcher circuit, sampler), then by filtering the 44.1 kHz frequency and other unnecessary noise by a low-pass filter. The signal obtained at this time is output as the analog audio signal.

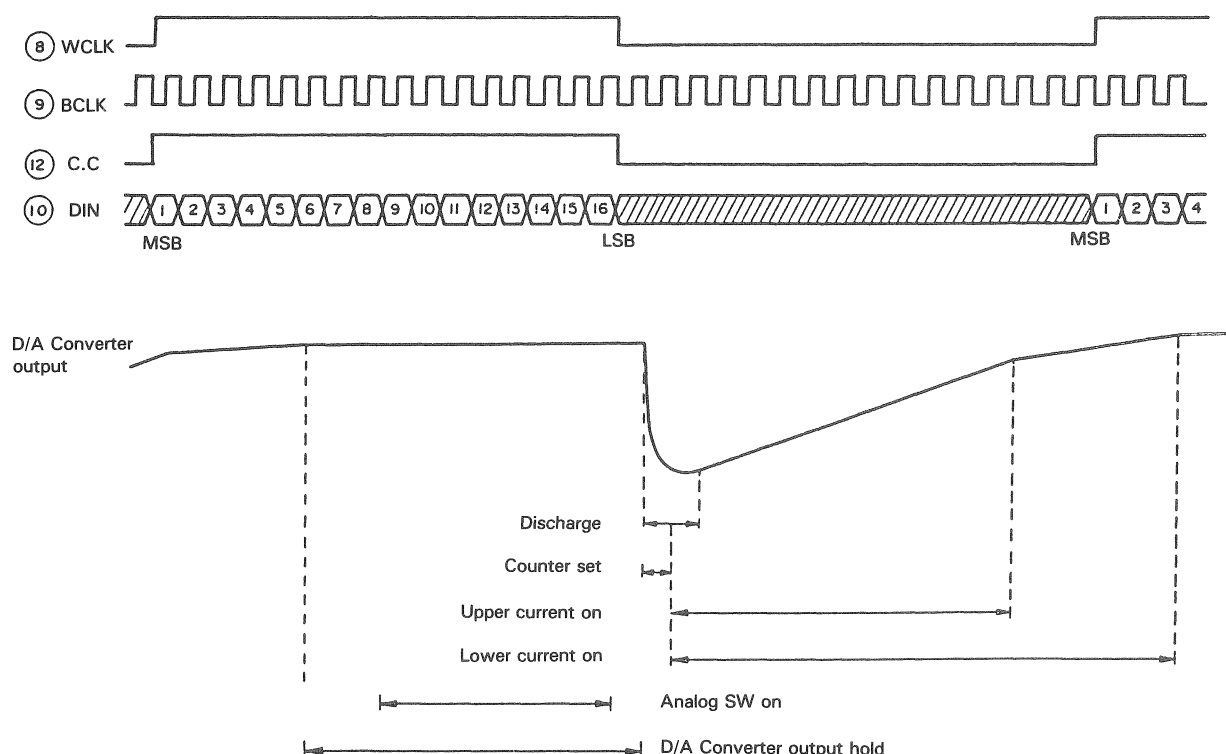


Fig. 2-3

2-1-6 Focusing and Tracking Servo

1) Tracking servo

The size of a data pit on the disc is 0.8 to 3.3 μm long and 0.4 μm wide, and the interval between tracks is 1.6 μm . When the disk is played, the track position may be shifted horizontally due to eccentricity or mechanism play, by an error of 0.1 mm with respect to the true circle. However, there are $100/1.6 = \text{approx. } 62$ tracks within the 0.1 mm difference.

In order to read data continuously during normal play mode, the same tracks have to be traced in order. The tracking servo is used to ensure this operation.

During search (kicking):

In modes other than normal play, there are cases in which a pulse is supplied to the tracking servo to force the pickup to trace same track continuously (pause mode) or to force the pickup to trace more than one track per one disc rotation (FWD and BWD modes).

2. DESCRIPTION OF FUNDAMENTALS CIRCUIT

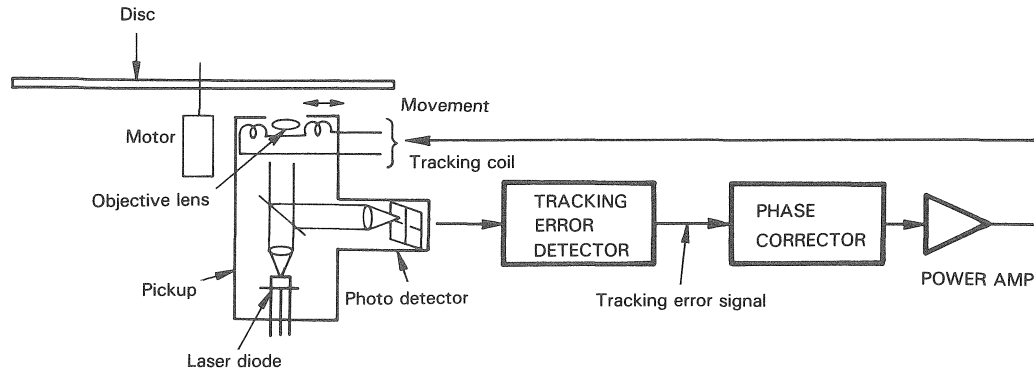


Fig. 2-4

2) Focusing servo

The field of depth (in which the image can be focused correctly) of the objective lens of the pickup is 1 to 2 μm . However, while the disc is rotating, there is an approx. 0.3 mm up/down movement due to warp or characteristics acquired in fabrication (supposing that the disc is rotating on a horizontal plane), and data cannot be read out if the pit surface moves out of the depth of field. The focusing servo is used to maintain the correct focus while a disc is played.

The focus search operation is performed in the beginning of play to find the correct focal point. This operation is carried

out by supplying a sawtooth wave of a few hertz to the focusing servo amp, in order to move the pickup's objective lens from far to near the disc and to find the correct focal point which enables the pickup to output correct RF signal. By switching the input signal to the focusing servo from the sawtooth wave to the focus error signal, a servo loop is formed and the objective lens can be moved so that the laser light is always focused on the pit surface.

The continuous output from the pickup is obtained by the above procedure.

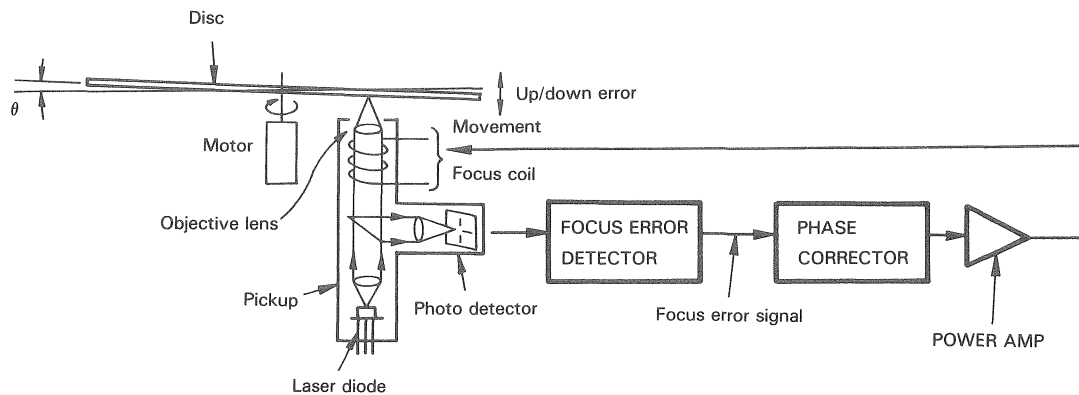


Fig. 2-5

2-1-7 CLV SERVO

The speed of data input to the jitter memory is proportional to the disc motor speed. The CLV servo functions to control the speed of the disc motor at a rate constant to the readout speed of data supplied to the D/A converter.

In other words, while a quartz-lock turntable regulates the FG frequency to a constant value, the CLV servo regulates the data output signal (WFCK) from the EFM decoder in place of

the FG frequency, so that it is equal to the reference signal (RFCK).

The speed control output (AFC) is supplied to the CLV circuit and amplified for the control of the disc motor speeds at its start or in operations requiring less accurate speed control, and a phase lock signal is supplied to the CLV circuit and amplified for the phase lock between the reference (RFCK) and compared (WFCK) signals.

2. DESCRIPTION OF FUNDAMENTALS CIRCUIT

2-1-8 Sled control servo

The objective lens in the pickup can trace only within a range of ± 1 mm in the data area. As a result, to cover all areas from the inner to outer circumferences, the sled control servo system moves the pickup itself so that the tracking servo can trace tracks correctly at the center of the objective lens tracking range (in radial direction).

The sled control servo operates to minimize the DC offset which is generated in the tracking servo output when the lens deviate from the center of the operating point.

When hundreds of tracks must be jumped in random search operation, etc., it is not only the objective lens which move, but the sled control servo system moves the pickup itself near the object point so as to quicken the following search operation.

2-1-9 Total control

A microprocessor puts in order the operations of the CD player, including the disc loading, pickup moving, time or track No. display, audio muting, operation key entry acceptances, execution of commands, etc.

3. DESCRIPTION OF ACTUAL CIRCUIT

3-1 OPTICAL SYSTEM AND RF AMPLIFIER

Description in this section is given separately for each of the blocks described in section 2, along the circuitry of the DP-770 shown on page 59.

The music data on the disc surface is read by the 3-beam spot pickup in the optical system block. Two of the three beams are used to generate the tracking error signal by detecting errors from the object track. The pickup incorporates four photodetectors for music data and two for tracking error detection. The electrical signal outputs from the four music data photodetectors are combined into two signals and sent to RF amp IC1. The two tracking error signal outputs are also input to IC1, their levels are compared, and the tracking error signal obtained by the comparison is output from TE (pin 17) to the tracking servo amp.

The focusing error signal is obtained by composing the two music data signals inside IC1. It is output from FE (pin 16) to the focusing servo amp.

The music signals are also composed inside IC1, amplified, and the square wave obtained is output from EFM (pin 20) to the signal processor IC.

In addition, the functions of IC1 include FOK signal for focus detection, MIR signal for the output of the tracking status, ASY signal for the DC component control of the EFM wave.

RF Amplifier IC1 (CX20109)

● CX20109 is a bipolar IC that includes an RF amplifier for optical system pickup output of 3-spot system developed for compact disc players as well as signal processing circuits such as focus, mirror, tracking and EFM comparator which are required for controlling the system.

3-1-1 Terminal connection diagram (Top view)

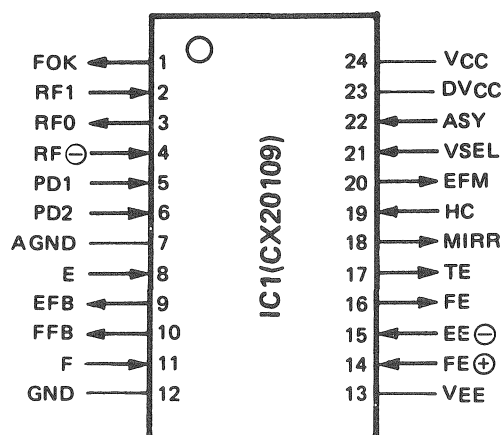


Fig. 3-1

3-1-2 Block diagram

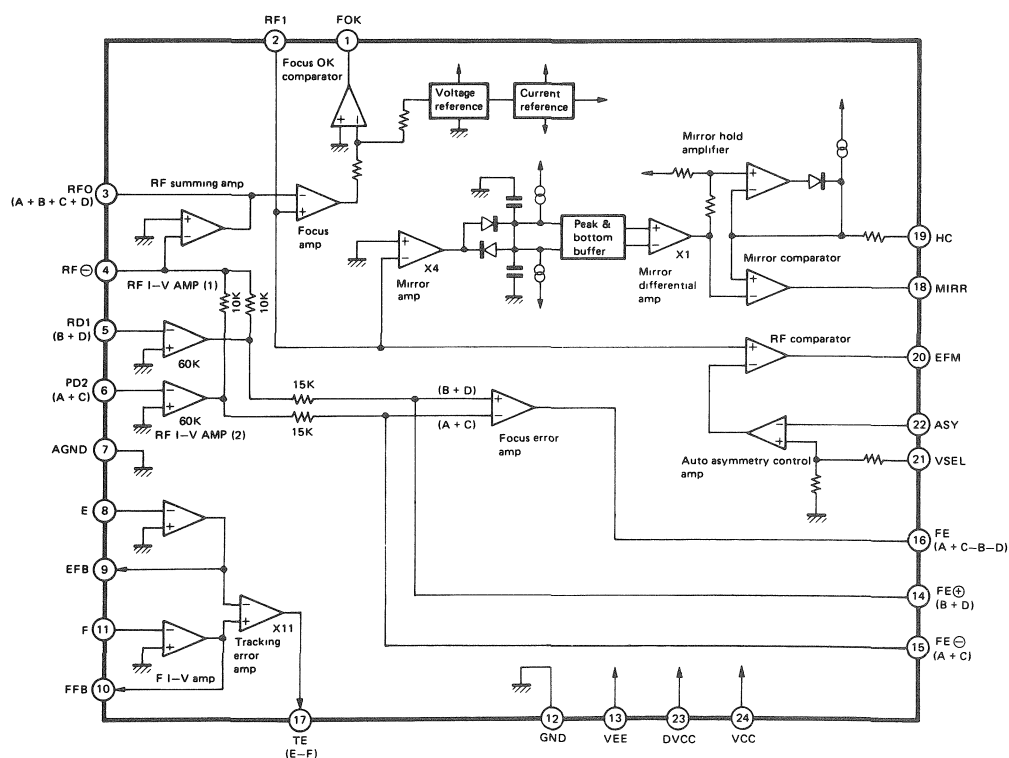


Fig. 3-2

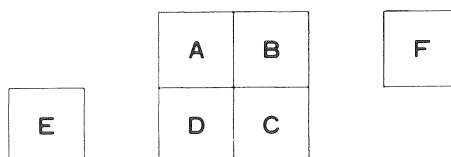
3. DESCRIPTION OF ACTUAL CIRCUIT

3-1-3 Explanation of functions of components

Terminal No.	Terminal name		Functions	DC volt
1	FOK	O	Focus, servo permit output. Active at comparator output "H". Connection of load resistance (PNP open collector).	0V
2	RFI	I	The output of the RF summing amplifier is coupled with C4 : 0.01 μ F.	0V
3	RFO	O	RF summing amplifier output. EYE pattern test point.	VRFO
4	RF $\ominus$	I	RF summing amplifier inverted input. Connection of feedback CR to ③ - ④ .	0V
5	PD1	I	RF I-V amplifier (1) inverted input. Current input as connected to PIN diode B + D (Note 1).	0V
6	PD2	I	RF I-V amplifier (2) inverted input Current input as connected to PIN diode A + C (Note 1).	0V 0V
7	A GND	-	Small signal analog system GND.	
8	E	I	E I-V amplifier inverted input. Current input as connected to PIN diode E (Note 1).	0V
9	EFB	O	E I-V amplifier output. Connection of feedback CR to ⑧ - ⑨ .	0V
10	FFB	O	F I-V amplifier output. Connection of feedback CR to ⑩ - ⑪ .	0V
11	F	I	F I-V amplifier inverted input. Current input as connected to PIN diode F (Note 1).	0V
12	GND	-	GND	0V
13	VEE	-	Negative power supply.	-5V
14	FE $\oplus$	I	Focus error amplifier non-inverted input. Connection of low-pass RC.	0V
15	FE $\ominus$	I	Focus error amplifier inverted input.	0V
16	FE	O	Focus error amplifier output. Connection of feedback CR to ⑮ - ⑯ .	VFEO
17	TE	O	Tracking error amplifier output.	VTEO
18	MIRR	O	Mirror output comparator output (active at "H"). Connection of load resistance (PNP open collector).	0V
19	HC	I	Mirror hold condenser (C9 : 0.033 μ F) connection terminal.	-2V
20	EFM	O	EFM output comparator output.	4.1V (OPEN)
21	VSEL	I	Terminal for setting reference input level of auto asymmetry control amplifier.	+ 5V
22	ASY	I	Auto asymmetry control input	-
23	DVcc	-	EFM comparator system positive power supply.	+ 5V
24	Vcc	-	Positive power supply.	

Table 3-1

Note 1 : Pattern of photodetector



3. DESCRIPTION OF ACTUAL CIRCUIT

3-2 PLL, EFM Decoder, etc

The description of multifunction LSI IC8 will be given as a whole, without separating its various functions into sub-items.

The EFM signal output from the RF amp consists of bit-serial data, and a sync clock pulse is required to decode it into the original data having 16 bits per word. In addition, because the EFM data handles data frames which include several words of data in each of them, it is always necessary to detect the beginning of each frame. A PLL circuit is incorporated in IC8 for the synchronization between the EFM signal bits and sync clock. An L-C type resonance circuit is connected across VCOO and VCOI, and the capacitance of external C is varied by phase comparator output PDO to generate readout clock PLCK which is synchronized with the EFM signal. The EFM and PLCK signals are both supplied to the frame sync detector to detect the beginning of each frame, and the 14-channel bits are decoded by the EFM demodulator into 8 bits, which are output via data buses DB01 to DB08 to be temporarily stored in external memory. The EFM signal holds the Q data, which is present in the user's bits immediately after the frame sync signal. The Q data contains the timing information concerning the position where the data is read out from the disc at a certain time, and is output from IC8 via SUBQ.

Each timing information can be obtained from 98 frames of data. These 98 frames form one "large frame", and the beginning of each large frame is indicated by the SCOR level going "H".

Whether there is error in the Q data read out from one large frame or not is indicated by the level of CRCF. ("L" indicates error.)

• Digital signal processing IC (CX23035)

3-2-1 Functions

CX23035 is an LS1 for processing digital signals of a compact disc player. It provides the following functions.

- Reproducing of bit clock by EFM-PLL circuit
- Demodulation of EFM data
- Detection, protection and interpolation of frame synchronizing signals
- Error detection, correction
- Interpolation by mean value or holding of previous value
- Demodulation of sub code signals, detection of errors in sub code Q
- CLV servo of disk motor
- Tracking counter of 8 bits
- CPU interface by serial bus

3-2-2 Internal block diagram

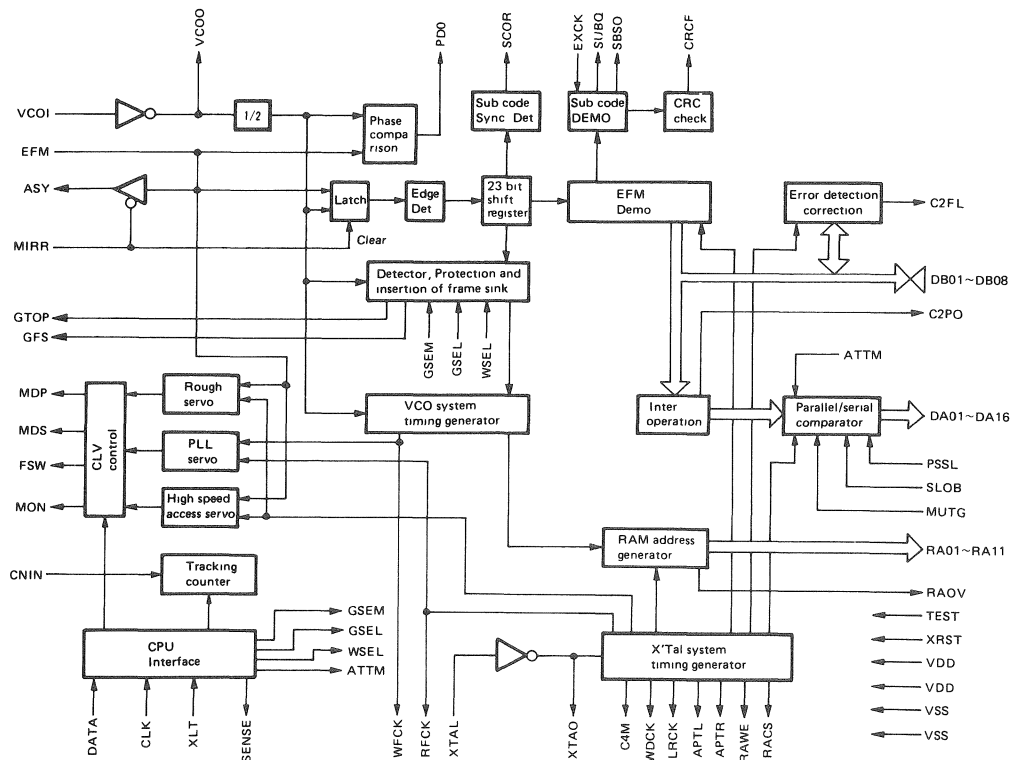


Fig. 3-3

3. DESCRIPTION OF ACTUAL CIRCUIT

3-2-3 Typical application circuits

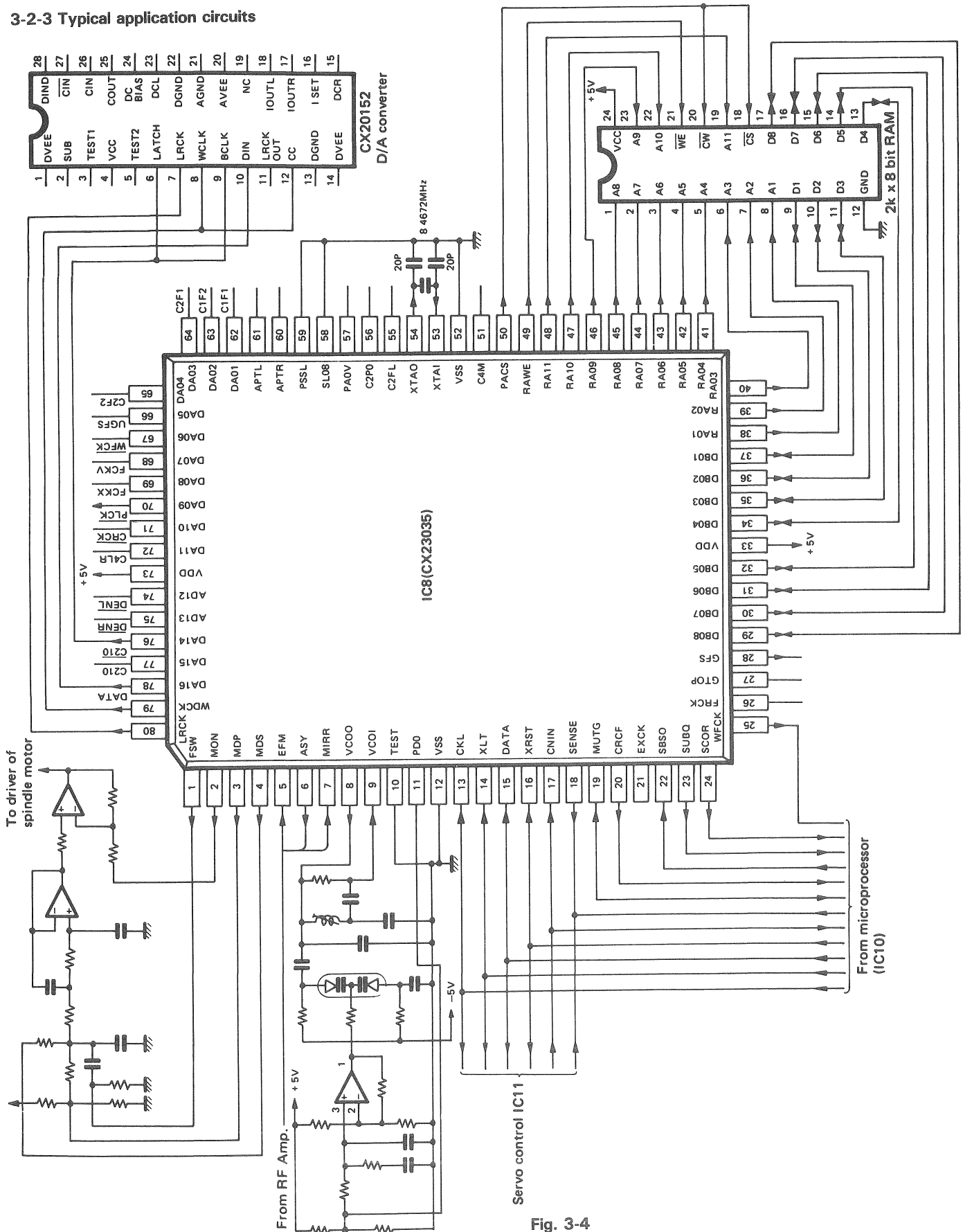


Fig. 3-4

3. DESCRIPTION OF ACTUAL CIRCUIT

3-2-4 Explanation of terminals

Terminal No.	Terminal name	I/O	Function
1	FSW	O	Time constant switching output of output filter of spindle motor.
2	MON	O	ON/OFF control output of spindle motor.
3	MDP	O	Drive output of spindle motor. Rough speed control in CLV-S mode and phase control in CLV-P mode.
4	MDS	O	Drive output of spindle motor. Speed control in CLV-P mode.
5	EFM	I	EFM signal input from RF amplifier.
6	ASY	O	Output for controlling the slice level of EFM signal.
7	MIRR	I	MIRROR input from RF amplifier.
8	VCOO	O	VCO output. $f = 8.6436\text{MHz}$ when locked to EFM signal.
9	VCOI	I	VCO input.
10	TEST	I	(0V)
11	PD0	O	Phase comparison output of EFM signal and VCO/2.
12	Vss	—	GND (0V)
13	CLK	I	Serial data transmission clock input from CPU. Data is latched at rising edge of a clock.
14	XLT	I	Latch input from CPU. Data (serial data from CPU) from the 8 bit shift register is latched in each register.
15	DATA	I	Serial data input from CPU.
16	XRST	I	System reset input. Reset at "L".
17	CNIN	I	Input of tracking pulse.
18	SENSE	O	Output of internal status in correspondence to the address.
19	MUTG	I	Muting input. In the case where ATTM of internal register A is "L", normal status when MUTG is "L" or soundless state when it is "H".
20	CRCF	O	Output of result of CRC check of sub code Q.
23	SUBQ	O	Sub code Q output.
24	SCOR	O	Sub code sync SO + SI output.
25	WFCK	O	Write Frame Clock output. $f = 7.35\text{kHz}$ when the frame sync is locked.
28	CFS	O	Output of display of lock status of frame sync.
29	DB08	I/O	Data terminal of external RAM. DATA 8 (MSB)
30	DB07	I/O	Data terminal of external RAM. DATA 7
31	DB06	I/O	Data terminal of external RAM. DATA 6
32	DB05	I/O	Data terminal of external RAM. DATA 5
33	VDD	—	Power supply (+ 5V)
34	DB04	I/O	Data terminal of external RAM. DATA 4
35	DB03	I/O	Data terminal of external RAM. DATA 3
36	DB02	I/O	Data terminal of external RAM. DATA 2
37	DB01	I/O	Data terminal of external RAM. DATA 1 (LSB)
38	RA01	O	Address output of external RAM. ADDR01 (LSB)
39	RA02	O	Address output of external RAM. ADDR02
40	RA03	O	Address output of external RAM. ADDR03
41	RA04	O	Address output of external RAM. ADDR04
42	RA05	O	Address output of external RAM. ADDR05
43	RA06	O	Address output of external RAM. ADDR06
44	RA07	O	Address output of external RAM. ADDR07
45	RA08	O	Address output of external RAM. ADDR08
46	RA09	O	Address output of external RAM. ADDR09
47	RA10	O	Address output of external RAM. ADDR10
48	RA11	O	Address output of external RAM. ADDR11 (MSB)
49	RAWE	O	Write Enable signal output to external RAM. (active at "L").
50	RACS	O	Chip select signal output to external RAM. (active at "L").

Table 3-2

3. DESCRIPTION OF ACTUAL CIRCUIT

Terminal No.	Terminal name	I/O	Function
52	Vss	—	GND (0V)
53	XTAL	I	X'tal oscillation circuit input. f = 8.4672MHz
54	XTAO	O	X'tal oscillation circuit input. f = 8.4672MHz
58	SLOB	I	Audio data output code switching input. 2's complement output at "L".
59	PSSL	I	Audio data output mode switching input. Serial output at "L".
70	PLCK	O	DA09 output when PSSL = "H". $\overline{\text{PLCK}}$ output when PSSL = "H".
76	$\overline{\text{C21O}}$	O	DA14 output when PSSL = "H". $\overline{\text{C21O}}$ output when PSSL = "H".
78	DATA	O	DA16 (MSB of parallel voice data) when PSSL = "H". DATA output when PSSL = "L".
79	WDCK	O	88.2kHz strobe signal output.
80	LRCK	O	44.1kHz strobe signal output.

Table 3-2

Note :

C1F1 : } Monitor output of error correction status
 C1F2 : } in C1 decode.
 C2F1 : } Monitor output of error correction status
 C2F2 : } in C2 decode.
 UGFS : Output of unprotected frame sync pattern.
 $\overline{\text{WFCK}}$: Inverted output of WFCK.
 FCKV : Output of WFCK/4 or WFCK/8.
 FCKX : Output of RFCK/4 or RFCK/8.

$\overline{\text{PLCK}}$: VCO/2 output. f = 4.3218MHz when locked to EFM signal.
 C4LR : 176.4kHz strobe signal.
 $\overline{\text{DENL}}$: Enable signal of L ch serial data.
 $\overline{\text{DENR}}$: Enable signal of R ch serial data.
 $\overline{\text{C21O}}$: Inverted output of C21O.
 C21O : Bit clock output. f = 2.1168MHz
 DATA : Serial data output of audio signal.

3. DESCRIPTION OF ACTUAL CIRCUIT

3-3 DEINTERLEAVING AND ERROR CORRECTION

While the data output from the EFM decoder is stored in external memory, data is arranged in the order of time by deinterleaving, and checked for errors. Correctable errors are corrected and, if there is an error that cannot be corrected, the error status is output from C2FL to the interpolater sec-

tion. The interpolater interpolates the data as required and sends it to the parallel/serial converter.

After converted into serial data, the music data is supplied together with LRCK, WDCK and C210 to D/A converter IC. The data flow and timing in this period are controlled by the RAM address generator and timing generator.

3-4 D/A CONVERTER AND AUDIO PROCESSOR BLOCK

• D/A converter (CX20152)

3-4-1 Internal block diagram

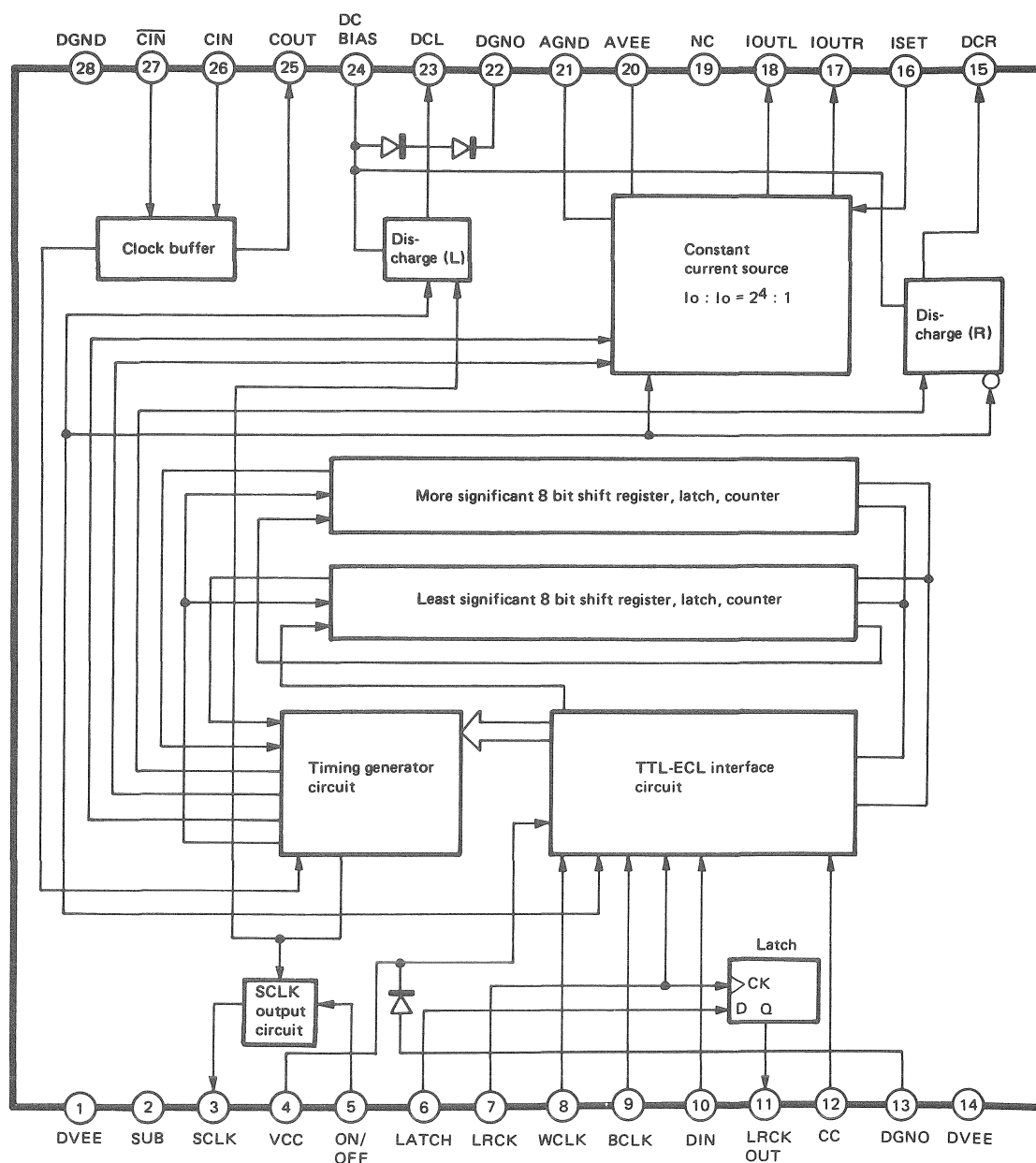


Fig. 3-5

3. DESCRIPTION OF ACTUAL CIRCUIT

3-4-2 Explanation of converting operation

● Data calling (BCLK, DIN, WCLK, LRCK)

Each data is a 16 bit serial signal and is of 2's complement form. Data are sequentially fed into the IC beginning with MSB in synchronization with rising edge of a bit clock (BCLK). (Data change occurs at falling edge of BCLK.)

When word clock (WCLK) is changed from high level to low level at 17th falling edge of BCLK, the 16 bit data is transmitted from the shift register to the latch by

this falling edge signal. In the case where CX20017 is used in the stereo mode, data of another channel is fed in beginning at the 17th BCLK.

Allocation of data in the stereo mode is such that R-ch data is called in while LRCK is of low level and L-ch data is called in while LRCK is of high level. Further, IOUTL, DCL operate when LRCK is of low level, and IOUTR, DCR operate only when LRCK is of high level.

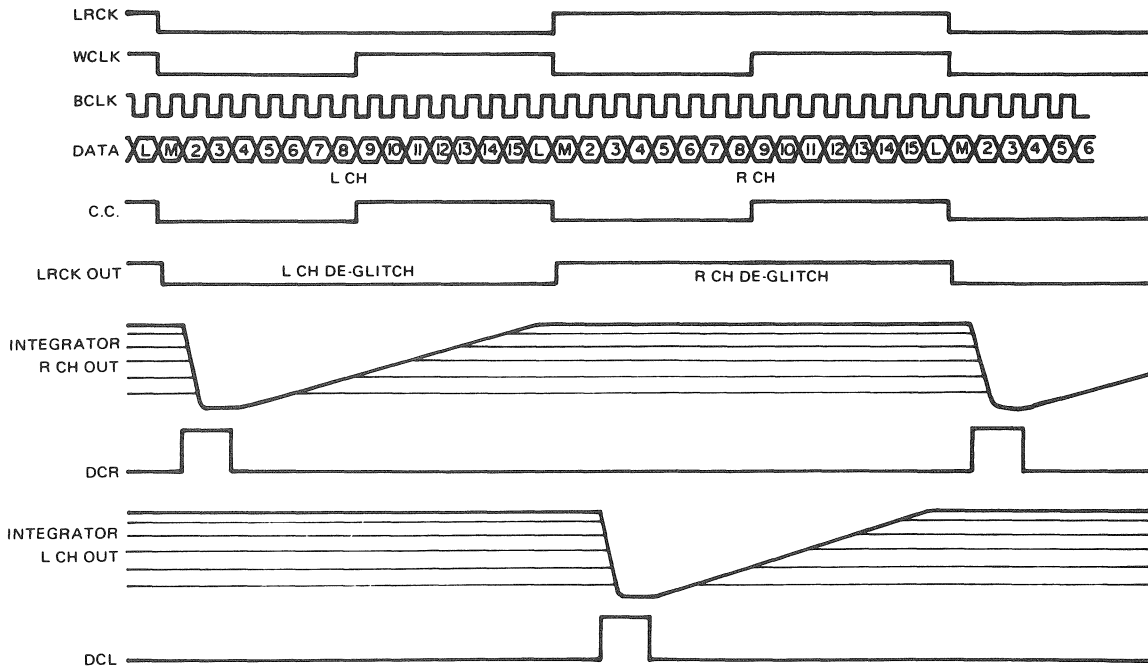


Fig. 3-6

● Converting operation (CC, LRCK, CIN, IOUTL, IOUTR, DCL, DCR)

All of the internal timing circuits are reset when the conversion command (CC) is set at high level and three or more clocks are fed through the clock input (CIN).

The internal timing circuits start operation CC is set at low level and a clock is fed through CIN after reset. The signals generated by operation of internal timing circuits are discharge signal, counter set signal and integration current start signal. The times of these signals are determined as follows from the clock period and number of clocks.

$$t_1 = 34 \times \tau_0$$

$$t_2 = 67 \times \tau_0$$

$$t_3 = 31 \times \tau_0$$

$$t_4 = 65 \times \tau_0$$

$$t_{5 \min} = 47 \times \tau_0 \quad (\text{when input data is } 01 \sim 1)$$

$$t_{5 \max} = 302 \times \tau_0 \quad (\text{when input data is } 10 \sim 1)$$

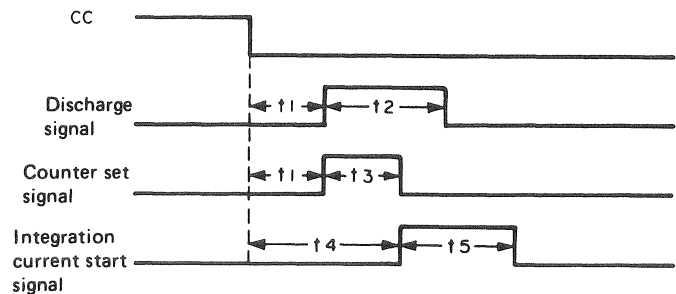


Fig. 3-7

3. DESCRIPTION OF ACTUAL CIRCUIT

The counter set signal is used for setting in counter the data that entered the latch, and it is not directed to the exterior. The discharge signal is directed out of DCL DCR. That is, it is directed out of DCL while LRCK is of low level or out of DCR while LRCK is of high level.

More significant current I_0 and less significant current i_0 flow out with an integration current start signal. The counter starts counting simultaneously with OFF of the discharge signal, and after finishing counting, it counts 11 offsets and issues a signal to stop the integration current. The value of t_5 varies between 0 and 255 depending on the input data value preset in the counter.

Therefore, the length of time required since CC level was changed to low level until end of integration, that is, conversion, is $(t_4 + t_5 \text{ max.})$ seconds at maximum. Further, as for this integration current, IOUTL is output while LRCK is of low level and IOUTR is output while LRCK is of high level, like the discharge signal.

● Setting of integration current (SET, IOUTL, IOUTR)

The integration current is determined by the constant current value fed from the ISET terminal. The relation is as follows.

$$IOUTL(R) = I_0 + i_0 = (4 + \frac{1}{64}) ISET$$

Where; i_0 is the integration current that is equivalent to 1LSB, and I_0 is the integration current that is equivalent to $2^8 \cdot \text{LSB}$.

● Operation of LRCK OUT (LATCH, LRCK, LRCK OUT)

The output of LRCK OUT is the output for driving the analog switch IC3 (UPD4053) to cut the output which was converted by CX20152 and the integrator as a PAM wave.

A conversion error occurs if jitter is present in the PAM wave. In order to absorb this jitter, therefore, D type flip-flop is incorporated, and LATCH input is used as its clock. This D type flip-flop causes a change in the output status in synchronization with raising edge a clock.

This LRCK OUT operates only when +5V is impressed to VCC. IC3 output level is $-3V \sim +3V$.

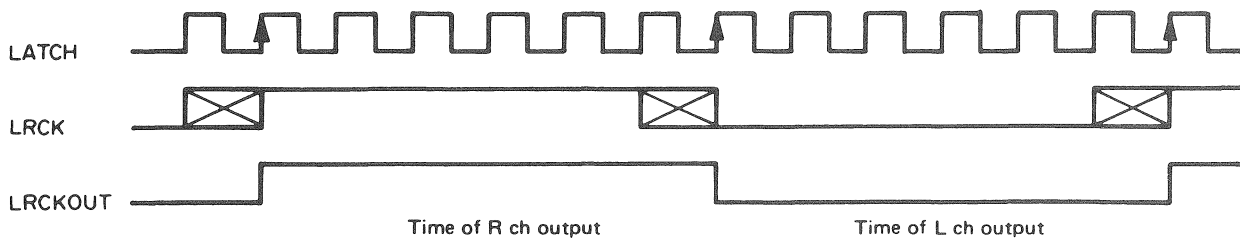


Fig. 3-8 Timing chart of LATCH, LRCK, LRCKOUT

● Clock input/output terminals (COUT, CIN, CIN)

The clock buffer is composed of a circuit that is equivalent to a general-purpose ECL logic circuit, and the input terminal is biased by an internal circuit. The ($\approx -1.3V$) output amplitude level is 0.8V

● Bias terminals (DVEE, SUB, DGND, VCC, AVEE, AGND, DC BIAS)

SUB is the substrate for the IC and is used at the potential common with ADVEE. The standard value of DVEE, AVEE is $-5.0V$. This CX20152 is used with the voltage at VCC terminal raised to +5V in order to cause the input to operated at $0 \sim +5V$. Further, LRCK OUT is output in this case as described earlier. BC BIAS is the bias circuit of the discharge signal output circuit.

As a current of about 2.5mA is required at standard value, power is supplied from IC15. The potential of this terminal is biased at 2Vf.

3. DESCRIPTION OF ACTUAL CIRCUIT

3-5 FOCUSING SERVO, TRACKING SERVO AND SLED CONTROL SERVO

The focusing and tracking error signals are output from the RF amp, passes through gain adjustment resistors, and goes to servo control IC11.

This IC uses the control code inputs from DATA terminal of its pin 8 for the control of operations required for the CD player, including the focus search, servo ON-OFF and track jumping in search operation.

The focusing and tracking control codes and their examples of applications are shown below.

● Servo signal processor (CX20108)

CX20108 is a bipolar IC developed for servo of compact disc (CD) players, and it provides the following functions.

- Focus control (search ON/OFF, gain control)
- Tracking control (servo ON/OFF, single track jump, multiple track jump, gain control, phase compensation control, brake circuit)
- Sled control (servo ON/OFF, fast forward, fast reverse)

Servo function of each of focus, tracking and sled as well as random access operation are realized through control by microcomputer. Furthermore, the serial data bus can be shared with CX23035.

3-5-1 Terminal connection diagram

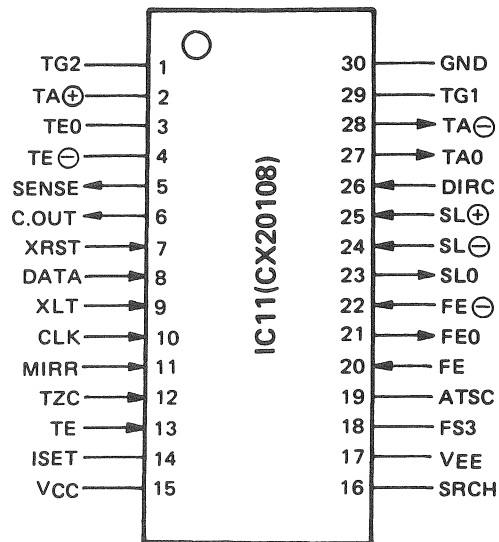


Fig. 3-9

3-5-2 Block diagram

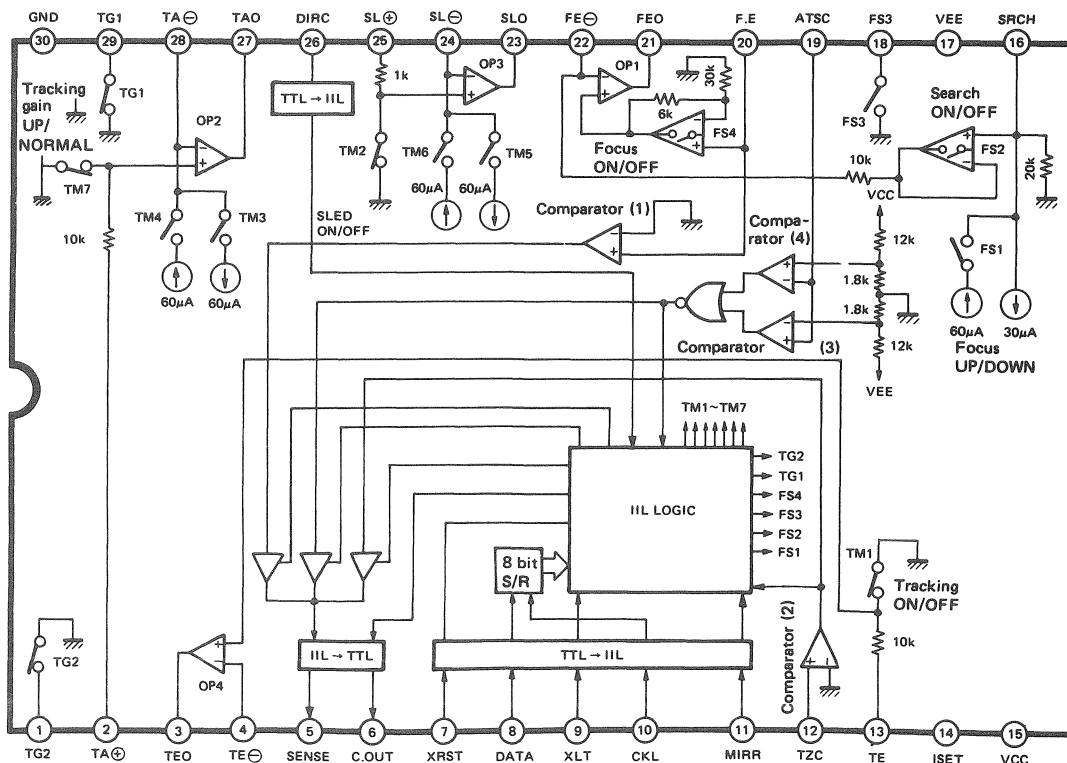


Fig. 3-10

3. DESCRIPTION OF ACTUAL CIRCUIT

3-5-3 Explanation of terminals

Terminal No.	Terminal name	I/O	Functions
1	TG2		Tracking amplifier gain switching terminal. GND level.
2	TA ⊕		Non-inverted input of operational amplifier 2.
3	TE0		Output of operational amplifier 4.
4	TE ⊖	O	Inverted input of operational amplifier 4.
5	SENSE	O	Output of SSP internal status that corresponds to ADDRESS of CPU → SSP. (Changes in accordance with ADDRESS content of internal serial register.) See Note 1.
6	C. OUT	O	Signal output for counting number of tracks at the time of high speed access.
7	XRST	I	All internal registers are cleared when CPU → SSP "L". Connected with CPU RESET. See Note 2.
8	DATA	I	Serial data transmission of CPU → SSP. Input is made from LSB. D0~D7.
9	XLT	I	Latch of serial data of CPU → SSP. (The contents of internal serial register are transmitted to each address decoded latch.) Transmission at "L". Change to "H" occurs immediately after execution because no edge trigger is produced.
10	CLK	I	CPU → SSP serial data transmission block. Data is read at falling. "H" level before and after transmission.
11	MIRR	I	Mirror signal input from RF amplifier.
12	TZC	I	Tracking error signal is input with C couple. The time constant is determined by one single track jump, but it is usually around 2kHz.
13	TE	I	Tracking error signal input.
14	ISST		Setting of current level for determining focus search voltage, tracking jump voltage and thread feed voltage.
15	Vcc		Power supply terminal. Normally -5V.
16	SRCH		The condenser for determining the time constant of charge/discharge waveform for focus search is connected.
17	VEE		Power supply terminal. Normally -5V.
18	FS3		Focus amplifier gain switching terminal. GND level.
19	ATSC		Such information that a mechanical shock was applied to the player is input. Simply, a tracking error is input through BPF. In this equipment it is connected to GND level and is not used.
20	FE	I	Input of focus error signal.
21	FE0	O	Output of operational amplifier 1.
22	FE ⊖	I	Inverted input of operational amplifier 1.
23	SL0	O	Output of operational output 3.
24	SL ⊖	I	Inverted input of operational amplifier 3.
25	SL ⊕	I	Non-inverted input of operational amplifier 3.
26	DIRC	I	Used at the time of one track jump. Normally "H". The direction of the track jump pulse is reversed with "L". Setting is made in the normal tracking mode by changing to "H". "L" for a fixed length of time with detection of activation, deactivation of TZC.
27	TA0	O	Output of operational amplifier 2.
28	TA ⊖	O	Inverted input of operational amplifier 2.
29	TG1		Tracking amplifier gain switching terminal. GND level.
30	GND		GND terminal of IC.

Note 1 : SENSE terminal output

Serial data upper 4 bits	ADDRESS content	SENSE terminal output	Explanation
0 0 0 0	FOCUS CONTROL	FZC	"H" when focus zero cross, Focus error voltage is 0V or higher Used at the time of FOCUS PULL operation
0 0 0 1	TRACKING CONTROL	AS	"H" when the ATSC input level exceeds the wind comparator level ($V_{TH} = \pm V_{cc} \times 13\%$) But this is not used in this equipment
0 0 1 0	TRACKING MODE	TZC	Judgement output of positive or negative of tracking zero cross, tracking error When used at the time of single track jump, DIRC is reduced to "L" on detection of TZC ↑, in FWD JUMP or on detection of TZC ↓ in REV JUMP

Table 3-3

Note 2 : Digital unit timing chart

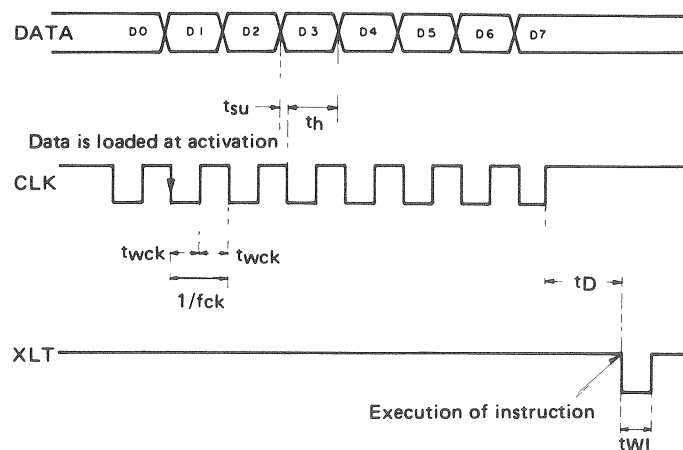


Fig. 3-11

3. DESCRIPTION OF ACTUAL CIRCUIT

3-5-4 Explanation of functions

The input data for causing this IC to operate is composed of 8 bits. It is hereinafter expressed in two hexadecimal digits like \$XX. (X is 0~F.)

Instructions to CX20108 are generally divided into three types, i.e., \$0X, \$1X and \$2X. Standard methods for use of these three types are explained below.

1) FS1, FS2 and focus search

The operation of FS1, FS2 is described next. (21), (22) etc. in Fig. 3—12 indicate terminal numbers of CX20108 (same hereinafter) OP1 is the operational amplifier for focus servo and the output of FS2 is connected to its inversion terminal. FS2 is such a switch that is ON and works as a usual voltage follower at the time of 1; and that its output is of high impedance at the time of 0. FS1 is a simple current switch which is OFF at the time of 1 and works to allow flow of $60\mu\text{A}$ at the time of 0. This value of $60\mu\text{A}$ is what is obtained when $240\mu\text{A}$ is fed to ISET (14) terminal. The voltage for focus search is produced using these FS1, FS2.

● \$0X (⑤ SENSE is "FZC")

This instruction is related to control of focus servo, and its bit composition is as follows.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	FS4	FS3	FS2	FS1

Four switches, i.e., FS1~FS4, are what are related to focus, and they correspond to D0~D3 respectively.

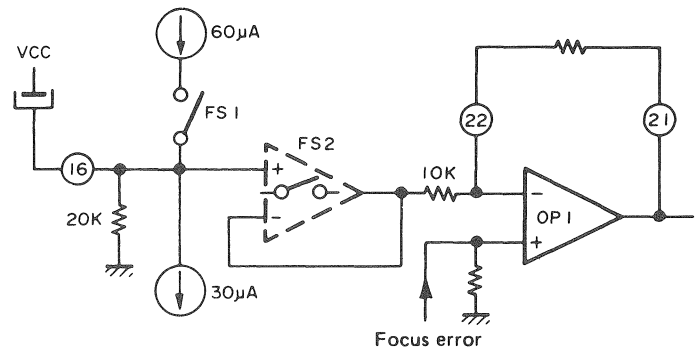


Fig. 3-12 Explanation of FS1, FS2

I \$00 (16) terminal is charged to $(60\mu\text{A} - 30\mu\text{A}) \times 20\text{k}\Omega = 0.6\text{V}$ when $\text{FS1} = 0$. Further, because $\text{FS2} = 0$, This voltage is not transmitted thereafter, and output (21) terminal is of 0V.

II \$02 FS2 only becomes 1 from the status described above. The output of FS2 is + 0.6V at this time and a negative output is directed to op2. This voltage level is specified as follows.

$$(60\mu\text{A} - 30\mu\text{A}) \times 20\text{k}\Omega \times \frac{\text{Resistance value between (21) - (22)}}{10\text{k}\Omega} \dots \dots \text{Expression (1)}$$

↑
At the time of $240\mu\text{A}$ (14)

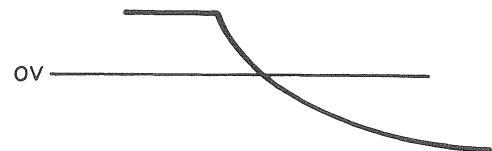


Fig. 3-13 Voltage at (16) terminal when $\text{FS1} = 0 \rightarrow 1$

III \$03 FS1 becomes 1 from the status described above and the current source of + $60\mu\text{A}$ is disconnected. Then, the CR's charge/discharge circuit is formed and the voltage at (16) terminal decreases as the time elapses as shown in Fig. 3—13.

This time constant is specified by internal $20\text{k}\Omega$ and external condenser C101 $22\mu\text{F}$.

It is possible to produce the focus search voltage by alternately instructing these II and III. (Fig. 3—14)

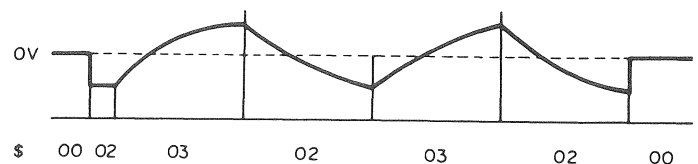
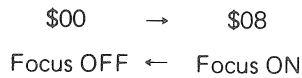


Fig. 3-14 Search voltage is produced by $\$02 \rightleftharpoons \03 (voltage at (16) terminal)

3. DESCRIPTION OF ACTUAL CIRCUIT

2) Explanation of FS4

This switch is a voltage follower (but the gain is 1.2 times) at the time of 1 and the output is open at the time of 0, like FS2 described earlier. This switch bears focus servo ON/OFF as located between focus error input 20 and input of OP1 described earlier.



3) Focusing procedure

The polarity is specified as follows for explanation.

- The lens searches in the direction of far → near to the disc.
- Output voltage ②① changes as negative → positive at this time.
- Further, the S curve of focus changes as shown in Fig. 3—15.

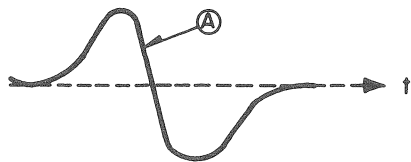


Fig. 3-15 S curve

Focus servo is applied with point ① shown in Fig. 3—15 as the actuation point. In general, the time when focus search is made and the focus servo switch is ON during passage through point ①. Furthermore, ANDing is made with focus OK signal (FOK) in order to prevent maloperation.

This IC is of such a design that what is obtained by comparing the focus error with 0V is output out of SENSE ⑤ terminal as the signal passing through point ① and is named as FZC (Focus Zero Cross).

Focus OK means a signal that indicates that focus is applied (may be applied, in this case), and it is output out of ① terminal of head amplifier IC1 (CX20109) in X29-1160-00.

when the above description is summarized, focus is applied in accordance with a timing chart like what is shown in Fig. 3—16.

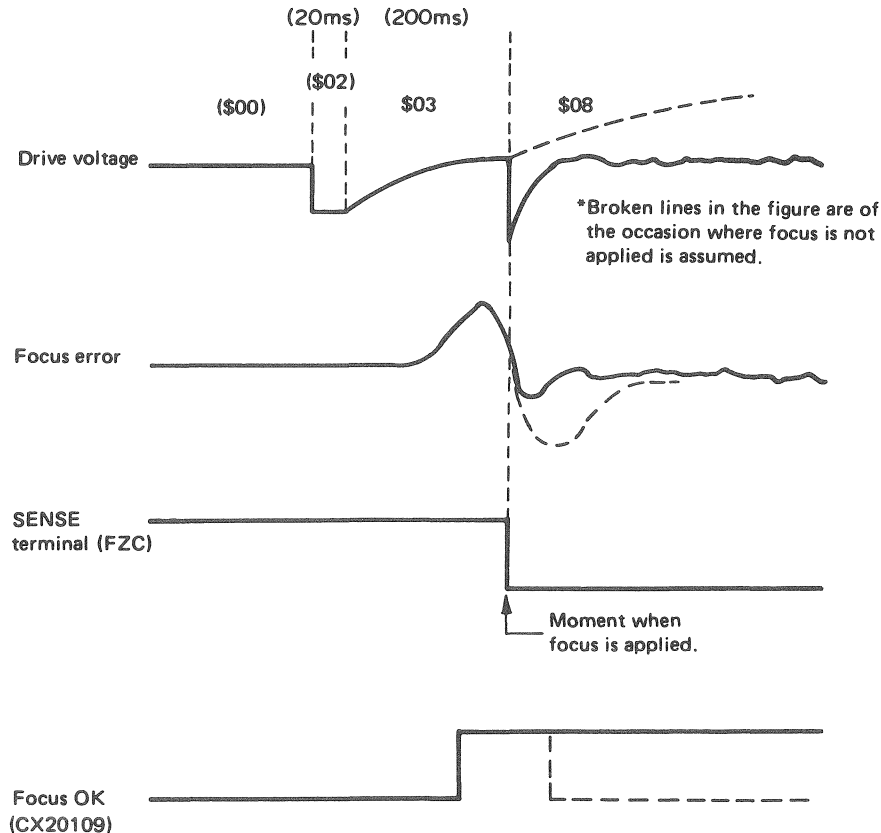


Fig. 3-16 Timing chart of focus OK

3. DESCRIPTION OF ACTUAL CIRCUIT

4) SENSE ⑤ terminal

As the output type is open collector of an NPN transistor, it is used with 22k Ω pull up. What is output varies by the input data. That is;

- FZC with \$0X
- "H" when the absolute value of the voltage applied to AS terminal exceeds 0.65V, or "L" when it is up to 0.65V, with \$1X.
- TZC with \$2X

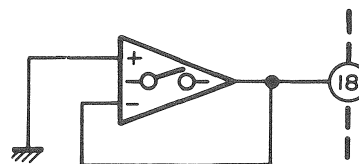


Fig. 3-17 FS3

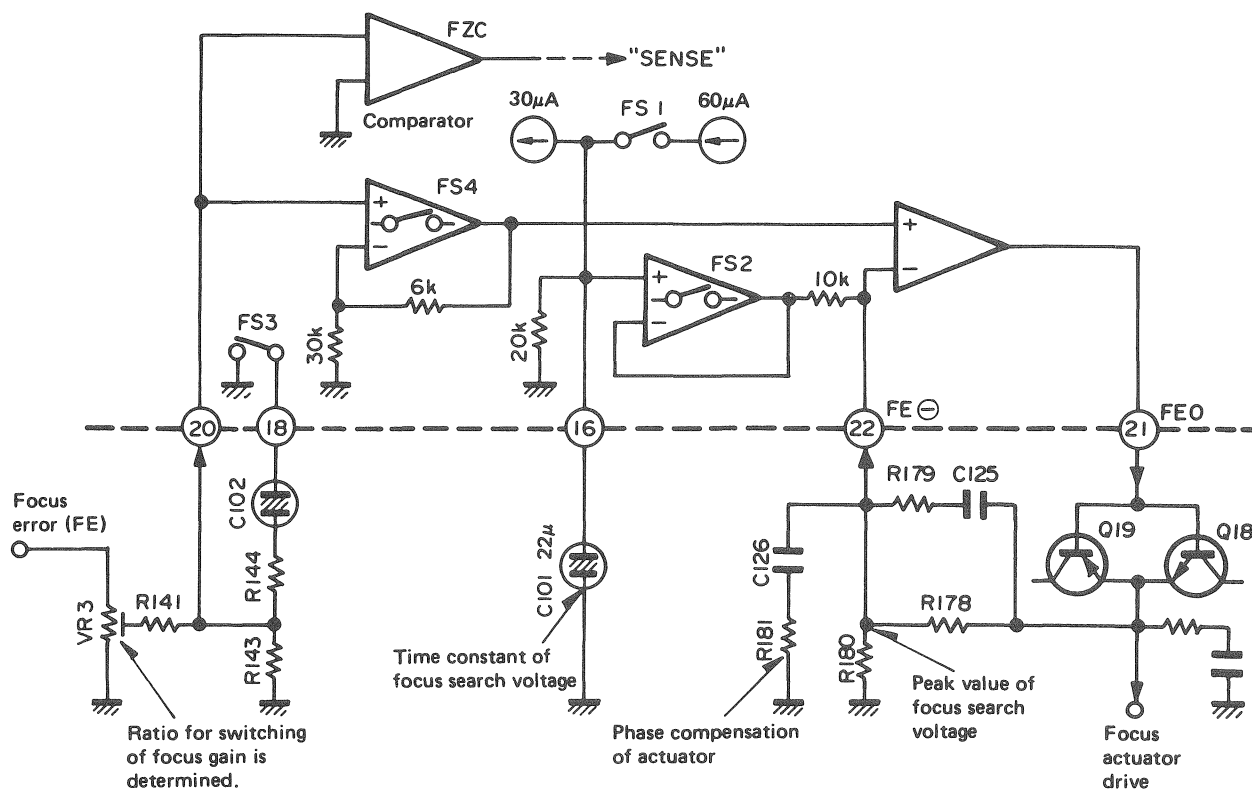


Fig. 3-18

Serial data	Hexa-decimal	Function	USAGE
FOCUS CONTROL		FS = 4321	
00000000	S00	0000	STOP
00000001	S01	0001	FOCUS SEARCH
00000010	S02	0010	
00000011	S03	0011	
00000100	S04	0100	
00000101	S05	0101	PLAY
00000110	S06	0110	
00000111	S07	0111	
00001000	S08	1000	
00001001	S09	1001	SEARCH
00001010	S0A	1010	
00001011	S0B	1011	
00001100	S0C	1100	
00001101	S0D	1101	
00001110	S0E	1110	
00001111	S0F	1111	

Table 3-4

3. DESCRIPTION OF ACTUAL CIRCUIT

● \$1X (5 SENSE is "AS")

This instruction is related to TG1, TG2 and brake circuit ON/OFF. The bit composition is as follows.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1		Brake circuit ON/OFF	TG2	TG1

1) TG1, TG2

The circuit type of these switches is same as that of FS3 shown in Fig. 3-17. However, the logic is opposite. High impedance is obtained with 1, and GND level is obtained with 0. The purpose of the switch is switching between UP/NORMAL of the tracking servo gain. One switch is used for switching of the gain and another for switching of the phase. A typical circuit is shown in Fig. 3-20.

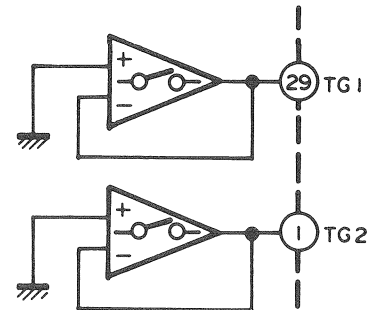


Fig. 3-19 TG1, TG2

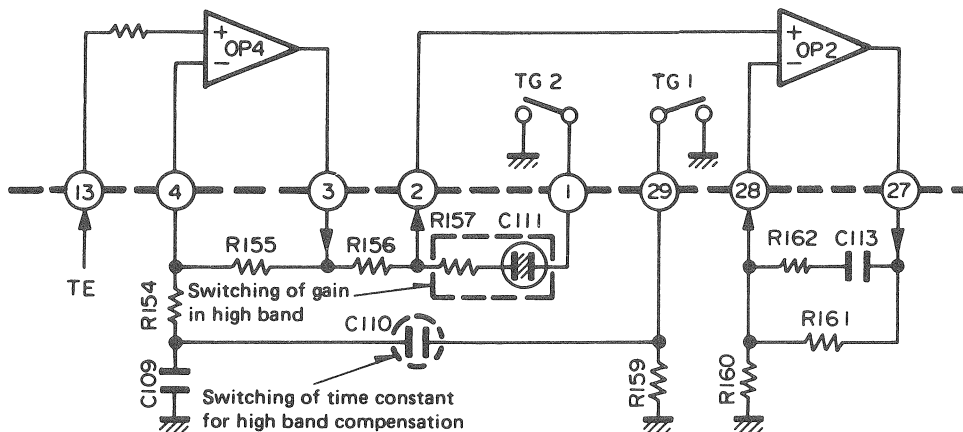


Fig. 3-20 Typical use of TG1, TG2

TRACKING CONTROL		D2	AS = 0 TG = 2 1	USAGE
00010000	S10	0	0 0	PLAY
00010001	S11	0	0 1	
00010010	S12	0	1 0	
00010011	S13	0	1 1	
00010100	S14	1	0 0	BRAKE
00010101	S15	1	0 1	
00010110	S16	1	1 0	
00010111	S17	1	1 1	SEARCH

Table 3-5

3. DESCRIPTION OF ACTUAL CIRCUIT

2) Brake circuit

The brake circuit is OFF (TM7 is open) when D2 = 0.

The brake circuit is ON (TM7 is open) when D2 = 1.

The brake circuit is explained next. See the section of 100 track jump and 10 track jump as for when the brake circuit is used.

The brake circuit is provided for preventing occurrence of such a phenomenon that only 10 tracks were jumped, even if it was intended to jump 100 tracks, due to the fact

that setting of the actuator is extremely inferior because the servo circuit exceeds the linear range after 100 track jump or 10 track jump. The phase relation between RF's envelope and tracking error is deviated by 180 degrees between the case where the actuator runs across tracks in the radial direction outward and the case where the same runs inward. The unnecessary portion of the tracking error is cut and brake is applied by making use of this nature, for improving setting of the actuator after track jump.

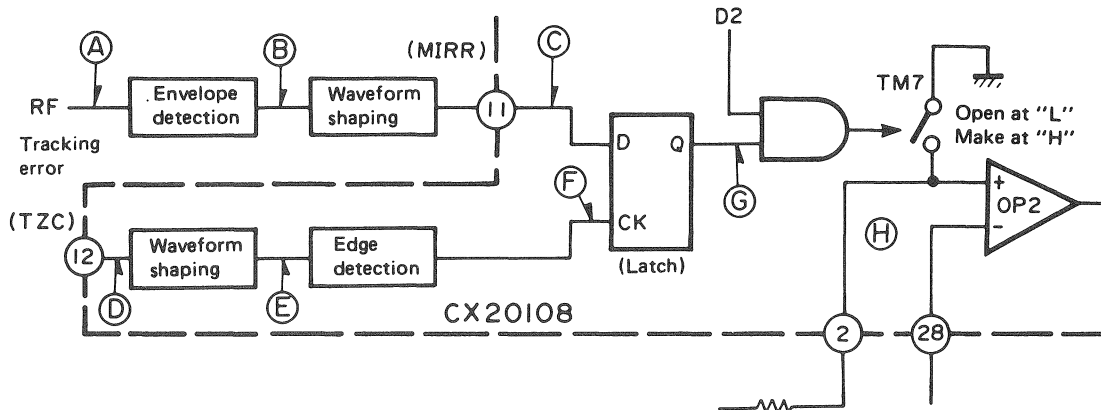


Fig. 3-21 Motion of TM7 (brake circuit)

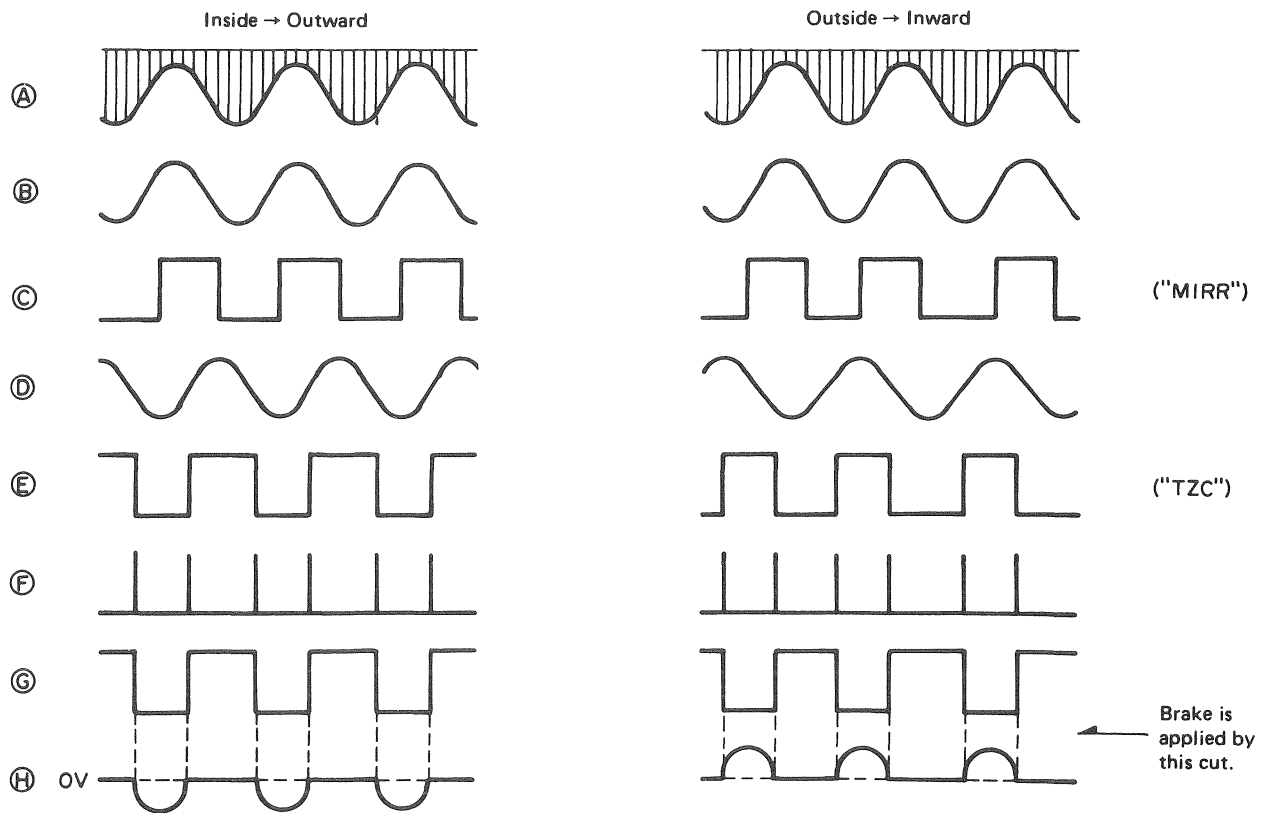


Fig. 3-22 Explanation of Fig. 3-21 (external waveform)

3. DESCRIPTION OF ACTUAL CIRCUIT

● \$2X (⑤ SENSE is "TZC")

This instruction is related to production of jump pulse and fast feed pulse at the time of ON/OFF of tracking servo and sled servo and also at the time of access.

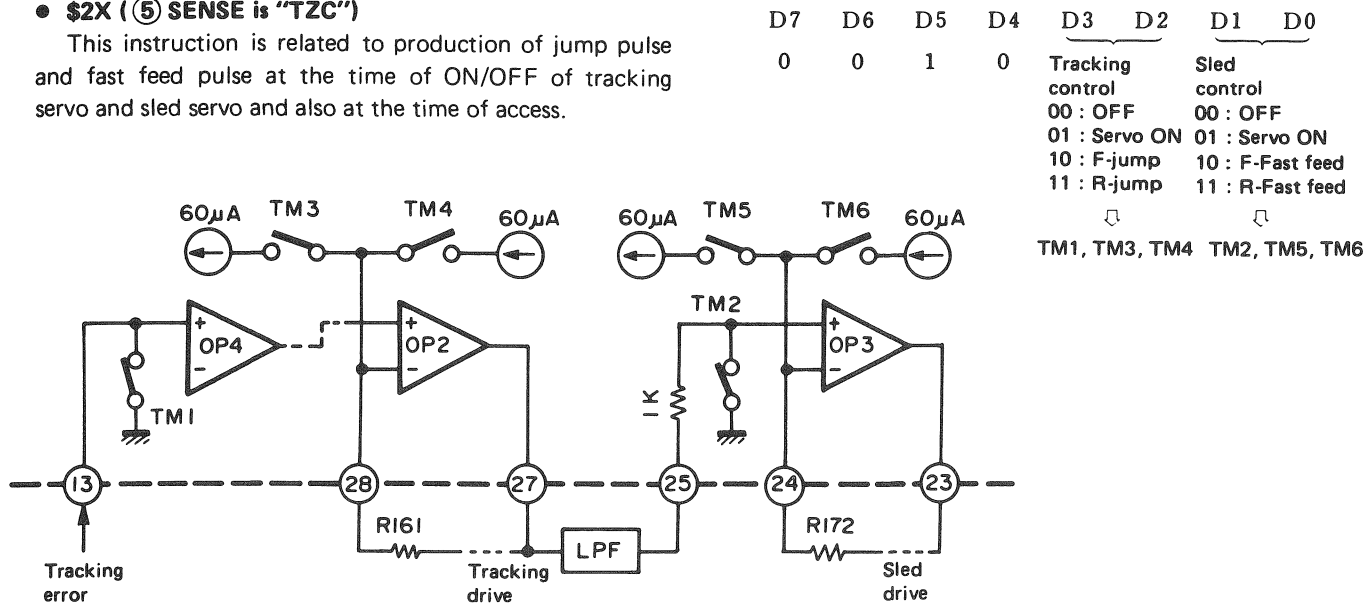


Fig. 3-23 TM1 ~ TM7

The circuit composition is shown in Fig. 3—23. TM1, TM2 make servo ON/OFF, and TM3~TM6 produce jump pulse and fast feed pulse. See truth value table for details.

Figure 60μA is observed in Fig. 3—23. This value is of the case where 240μA is fed to ISET (⑭) terminal like SF1. The circuit of (⑭) terminal is as shown in Fig. 3—24. Therefore, the potential is around (—) VEE +0.9V.

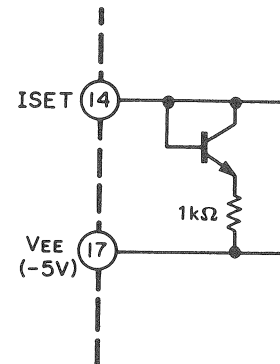


Fig. 3-24 ISET terminal

1) DIRC (②⑥) terminal and single track jump

1 track jump usually gives an acceleration pulse, and then observes the tracking error; gives deceleration pulses for a fixed length of time from the time when the tracking error ran across 0 point, and again turns ON the tracking servo. 100 track jump to be explained in the next paragraph is satisfactory if approximately 100 tracks are jumped, but 1 track jump should be absolutely 1 track jump. Therefore, such a complicated measure is taken.

Therefore, DIRC (Direct Control) terminal is provided for this IC in order to facilitate single track jump by its operation. That is, for performing single track jump using DIRC (DIRC is usually "H")

- An acceleration pulse is produced. (\$2C if REV; or \$28 if FWD)
- DIRC is changed to "L" by TZC ↓ (or TZC ↑). (⑤ SENSE is "TZC".) The polarity of the jump pulse is inverted and deceleration is applied.
- DIRC is changed to "H" after a fixed length of time. Both tracking servo and sled servo are ON automatically.

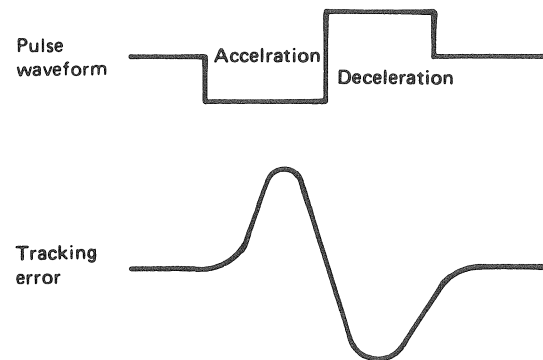


Fig. 3-25 Pulse waveform and tracking error of single track jump

3. DESCRIPTION OF ACTUAL CIRCUIT

2) 100 track jump

With this IC, basically it is not possible to change the amplitude of the jump pulse between 1 track jump and 100 track jump. (Because the value of the current input to ISET (14) terminal is fixed.)

Therefore, the amplitude is determined by 1 track jump and 100 track jump is controlled by time with the voltage remaining unchanged.

100 track jump is of smooth feed by jointly using sled fast feed (so-called "kick-off") besides drive of the tracking actuator. The length of this kick off is determined so that the access time is the minimum.

Brake circuit ON and tracking gain UP are made to stabilize the setting operation after the jump.

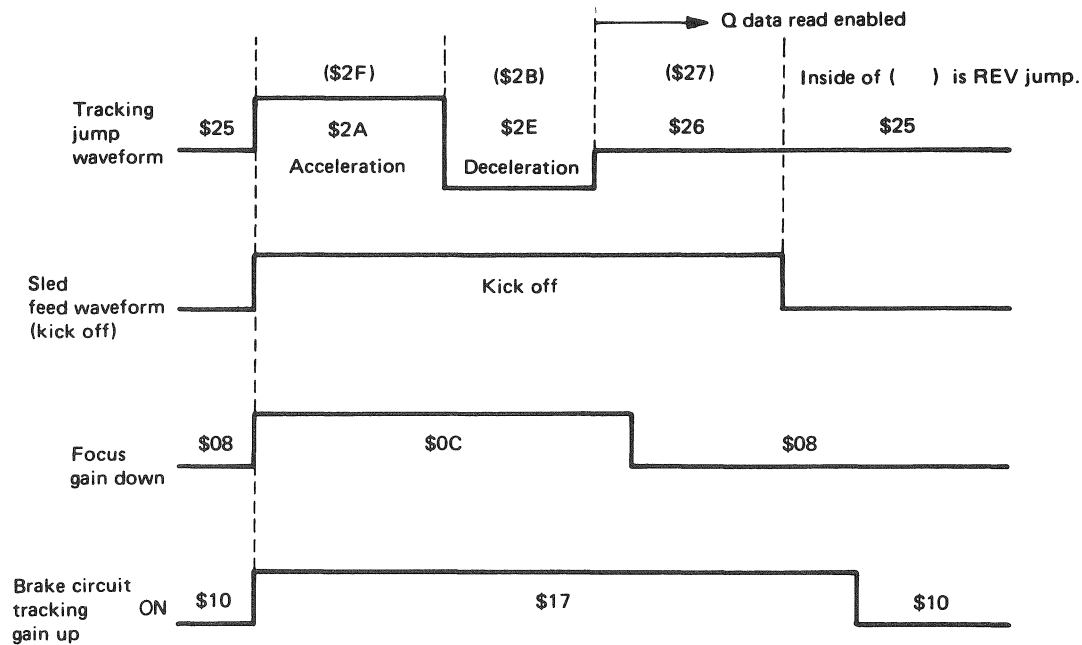


Fig. 3-26 100 track jump timing chart

3) 10 track jump

As this is intermediate between 100 and 1, the required number of tracks is set at a value that is close to 10, and therefore, the jump pulse width is determined by counting the number of jumped tracks.

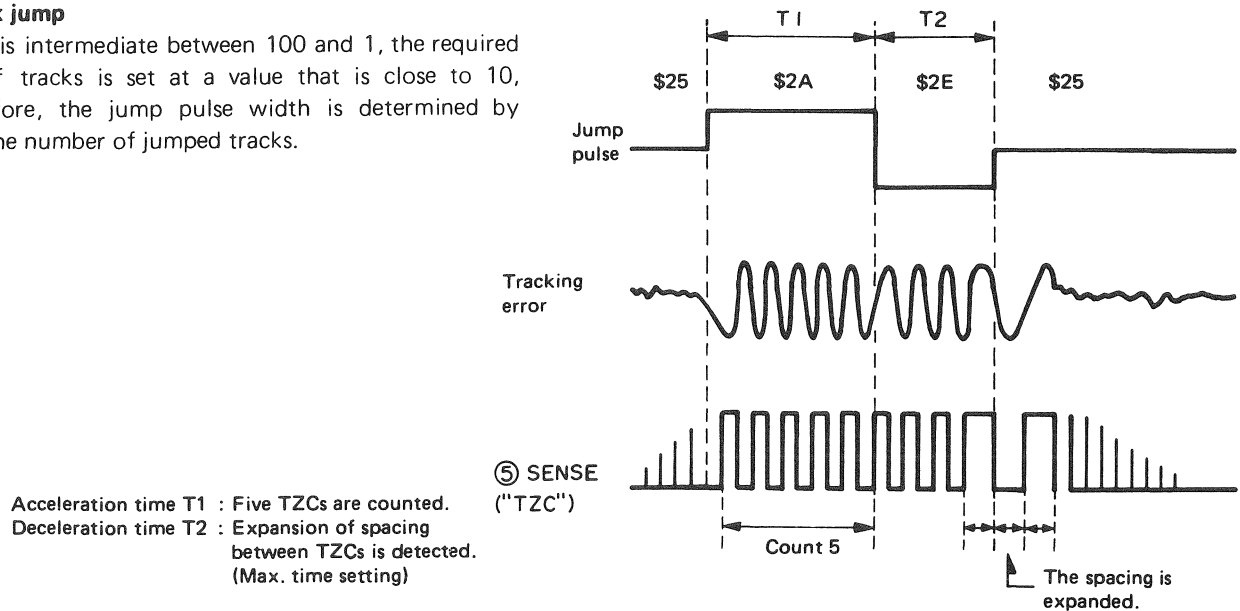


Fig. 3-27 10 track jump

3. DESCRIPTION OF ACTUAL CIRCUIT

4) Access by making joint use of 100, 10 and 1 track jumps

Jump pulses and kick off pulses (that is, \$2X relation) are set as described in the paragraph of \$2X and subsequent, and as for \$1X relation, instructions are output in a batch, as shown in Fig. 3—28.

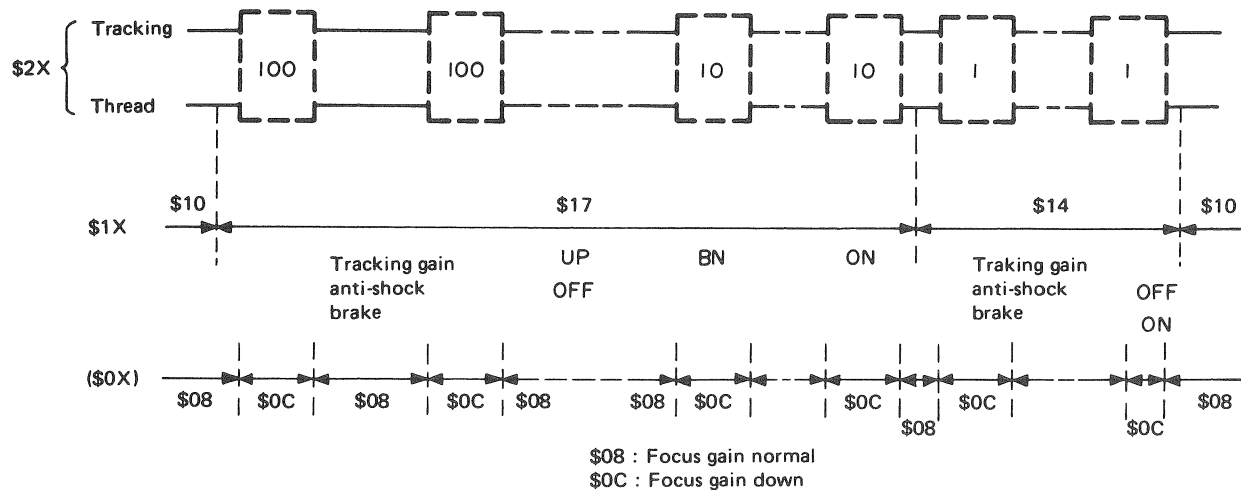


Fig. 3-28 Typical access time instruction codes

● How to use high speed access and Count Out ⑥

It is needless to say that access time for head search of a music and so forth is shorter. In the access using 100, 10, 1 track jump, however, about 4 seconds is the limit from the innermost periphery to the outermost periphery of the disc. It is because 100 track jump consumes more than 80% of the time, and it is possible to shorten the time if the length of time of this "major movement" can be shortened. As the distance from the current location to the destination can be learned from the TOC and the absolute time of the current location, rough feed is made for this distance.

Several methods are available as for the means to replace this distance. In general, it is the number of tracks divided by $1.6\mu\text{m}$, sled motor revolution (number of steps, if it is a stepping motor) or potentiometer's voltage, if provided.

C.OUT ⑥, which is a terminal exclusive for counting number of tracks is provided on this IC in order to make correspondence to counting of number of tracks. As this signal is what is obtained by latching MIRROR signal by the edge of T2C (that is, same as the signal used in the brake circuit), and therefore, even if tracking error signal, etc. include noise, such noise is ignored.

TRACKING MODE		DC = 1 TM = 654321	USAGE
00100000	S20	000000	STOP
00100001	S21	000010	
00100010	S22	010000	
00100011	S23	100000	
00100100	S24	000001	
00100101	S25	000011	PLAY
00100110	S26	010001	
00100111	S27	100001	
00101000	S28	000100	FWD KICK
00101001	S29	000110	
00101010	S2A	010100	
00101011	S2B	100100	
00101100	S2C	001000	BWD KICK
00101101	S2D	001010	
00101110	S2E	011000	
00101111	S2F	101000	

Table 3-6

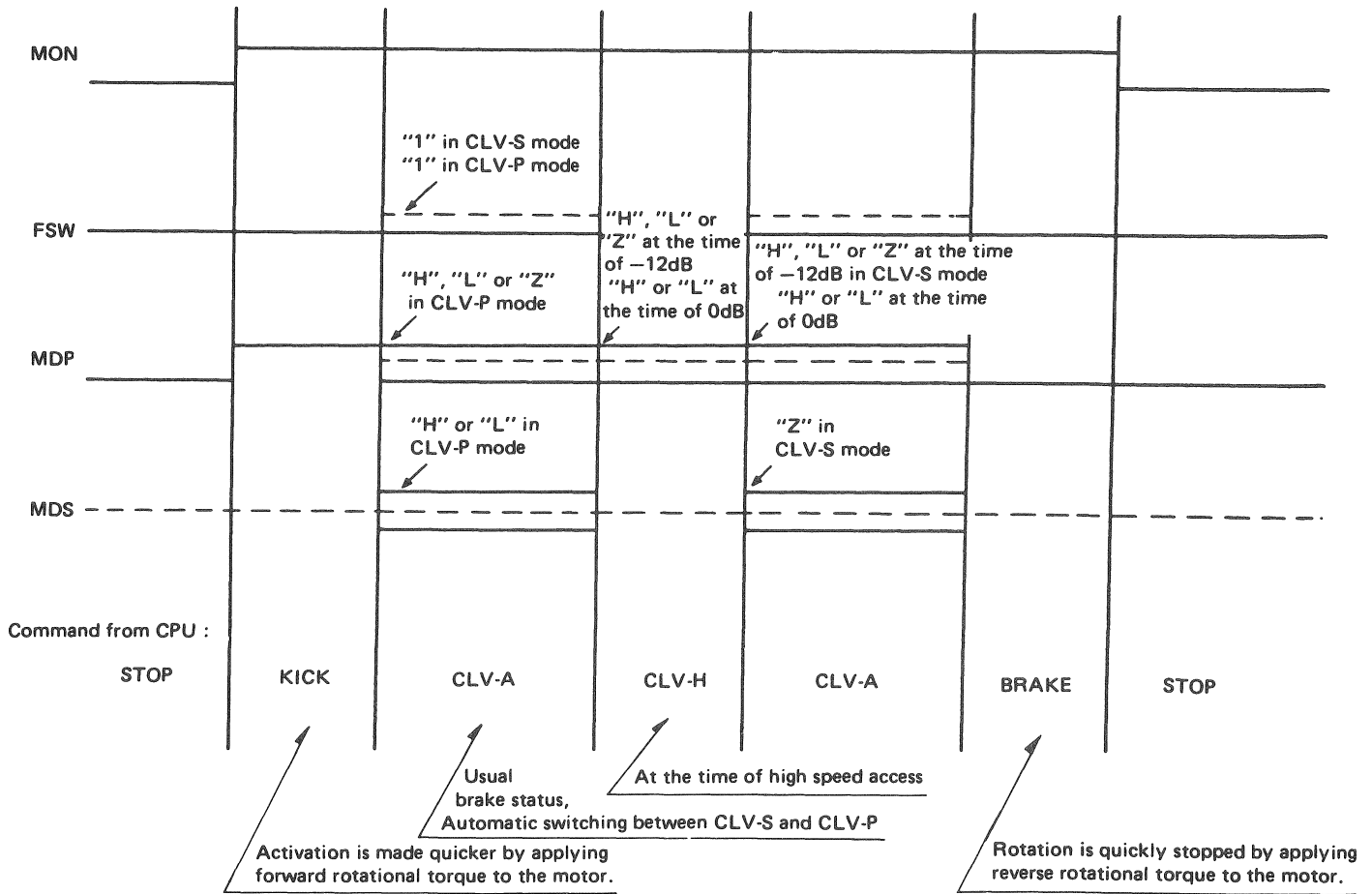
DC : DIRC input terminal

3. DESCRIPTION OF ACTUAL CIRCUIT

● CLV servo control

The spindle motor revolution is controlled with one selected out of the following seven modes in accordance with a command from the CPU. CLV is the abbreviation of Constant Linear Velocity. The output is composed of MDP terminal for controlling synchronization of velocity and phase, MDS terminal for controlling synchronization of velocity, FSW terminal for making selection of filter constant and MON terminal for controlling motor ON/OFF.

- 1) STOP : Register E = 0000'B (B means binary)
Mode for stopping the spindle motor.
MDP = FSW = MON = "L", MDS = "Z"
- 2) KICK : Register E = 1000'B
Mode for running the spindle motor in forward direction.
MDP = MON = "H", MDS = "Z", FSW = "L".
- 3) BRAKE: Register E = 1010'B
Mode for running the spindle motor in reverse direction.
MDP = FSW = "L", MDS = "Z", MON = "H".



Z : High impedance

Fig. 3-29 Typical control of spindle motor

*3) Register E

Mode	D3~D0	MDP terminal	MDS terminal	FSW terminal	MON terminal
STOP	0 0 0 0	L	Z	L	L
KICK	1 0 0 0	H	Z	L	H
BRAKE	1 0 1 0	L	Z	L	H
CLV-S	1 1 1 0	CLV-S	Z	L	H
CLV-H	1 1 0 0	CLV-H	Z	L	H
CLV-P	1 1 1 1	CLV-P	CLV-P	Z	H
CLV-A	0 1 1 0	CLV-S or CLV-P	Z or CLV-P	L or Z	H

Z : High impedance

Table 3-7 List of registers

3. DESCRIPTION OF ACTUAL CIRCUIT

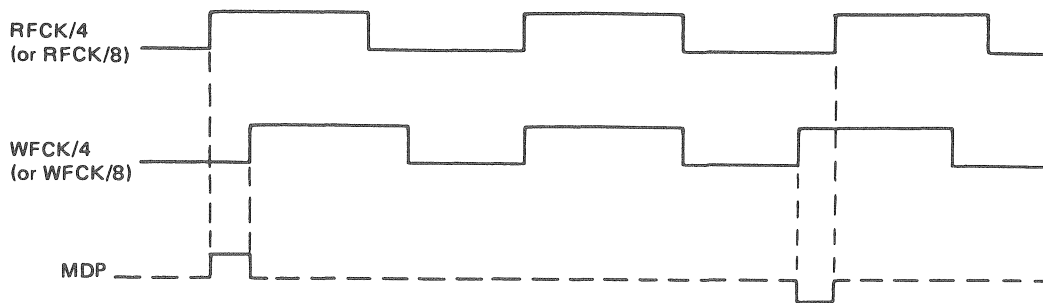
4) CLV-P : Register E = 1111'B

PLL servo mode.

Phase comparison of signals WFCK/4 and RFCK/4 or WFCK/8 and RFCK/8 is made, and output is made out of MDP terminal. "H" when WFCK has delayed, "L" when WFCK is fast, and "Z" when synchronized. When the period of $8.4672/2\text{MHz}$ is expressed at T and the length of time when WFCK is "H" is expressed at tHW, such a signal that is of "H" during (tHW-279T)

x 32 with 7.35kHz as a period and that is "L" during the remaining time is produced out of MDS terminal. MDS = "L" when $t\text{HW} \leq 279T$. MDS = "H" when $t\text{HW} \leq 297T$. When $280T \leq t\text{HW} \leq 296T$, the MDS terminal changes in 32T steps from 32T to 544T. When synchronized, for instance, that is, when $t\text{HW} = 288T$, a signal of 7.35kHz of DUTY 50% is produced. FSW = "Z", MON = "H".

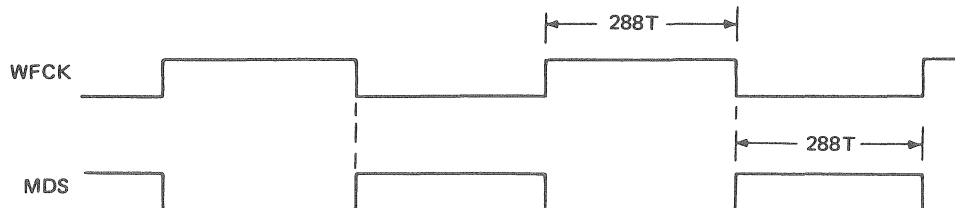
*MDP terminal



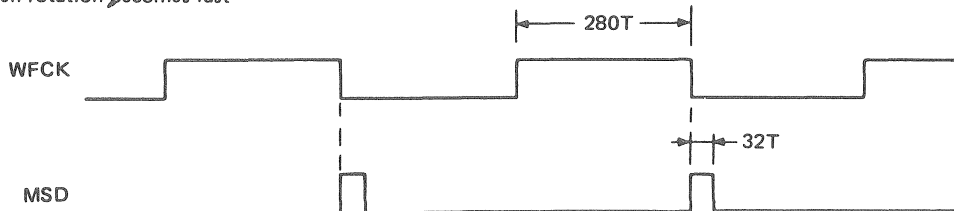
* MDS terminal (the period of 4.2336MHz is expressed as "T".)

Z : High impedance

(1) When rotating at specified velocity



(2) When rotation becomes fast



(3) When rotation becomes slow

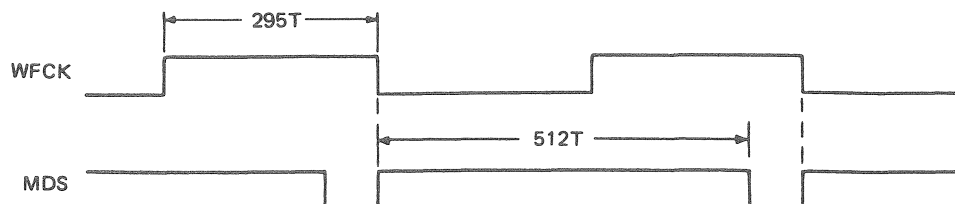


Fig. 3-30 Timing chart in CLV-P mode

3. DESCRIPTION OF ACTUAL CIRCUIT

5) CLV-S : Register E = 1110'b

Rough servo mode used at the time of start of rotation, at the time of track jump and also when the EFM-PLL circuit is unlocked due to another reason. When the period of VCO's oscillation frequency 8.6436MHz is expressed as "T", the pulse width of a frame synchronizing signal is "22T" during specified revolution, and it is the maximum pulse width in a period of RFCK. In practice, however, there are pulses having widths over "22T" due to drop-off of EFM signal due to other reasons, and the frame synchronizing signal cannot be correctly detected unless such pulses are removed. Therefore, the maximum value (peak) of the pulse width of EFM signal is detected (called peak hold) in the period of RFCK/2 or RFCK/4, than the minimum value in this peak is detected (called bottom hold) in the period of RFCK/16 or RFCK/32, and this value is used as the frame synchronizing signal. "L" is produced out of MDS terminal while the frame synchronizing signal is "21T" or less, "Z" when it is "22T", or "H" when it is "23T" or more.

Either 0dB or 12dB can be selected as its gain. MDS = "Z", FSW = "L", MON = "H".

6) CLV-H : Register E = 1100'B

Rough servo mode during high speed access. If the number of tracks from the innermost periphery to the outermost periphery is 2000 tracks and access over these tracks is made in 1 second, each mirror (place without pit) portion between tracks is of a signal of 20kHz, and is superposed on the EFM signal. When the above mentioned signal is input in the CLV-S mode, a mirror portion that is longer than the original frame synchronizing signal is detected as the peak value, and servo becomes unstable. In the CLV-H mode, therefore, the mirror portion is eliminated by making peak hold in the period of $8.4672/256\text{MHz}$ about 34kHz) instead of RFCK/2 or RFCK/4 and by making bottom hold in the period of RFCK/16 or RFCK/32 like in CLV-S mode, and thus the servo during high speed access is made stable. Other than the period for detection of the peak is same as CLV-S mode.

Pwmax : Pulse width after bottom hold

TB : Bottom hold period, RFCK/16 or RFCK/32

Z : High impedance

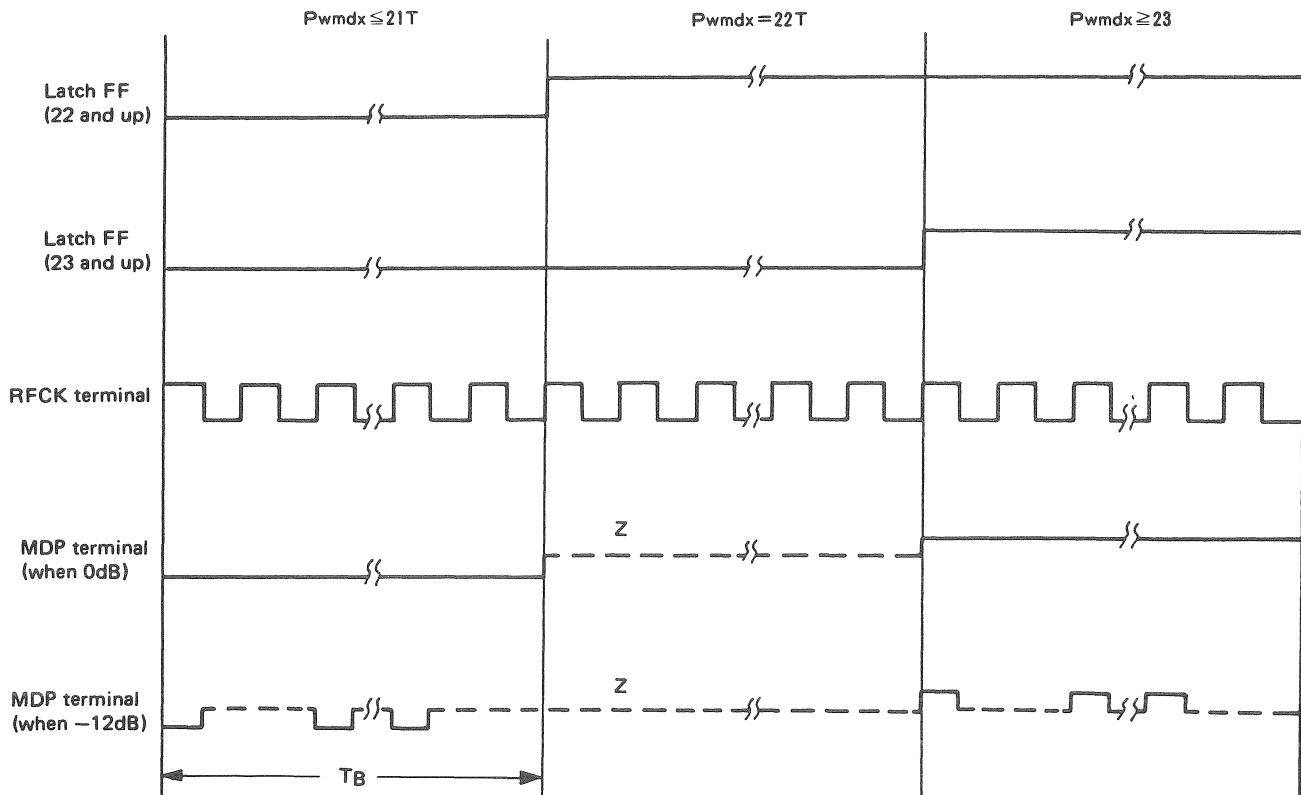


Fig. 3-31 Timing chart in CLV-S, CLV-H mode (1)

3. DESCRIPTION OF ACTUAL CIRCUIT

TP : RFCK/2 or RFCK/4 in the case of CLV-S,
F8M/256 in the case of CLV-H
TB : RFCK/16 or RFCK/32 in the case of
CLV-S, CLV-H

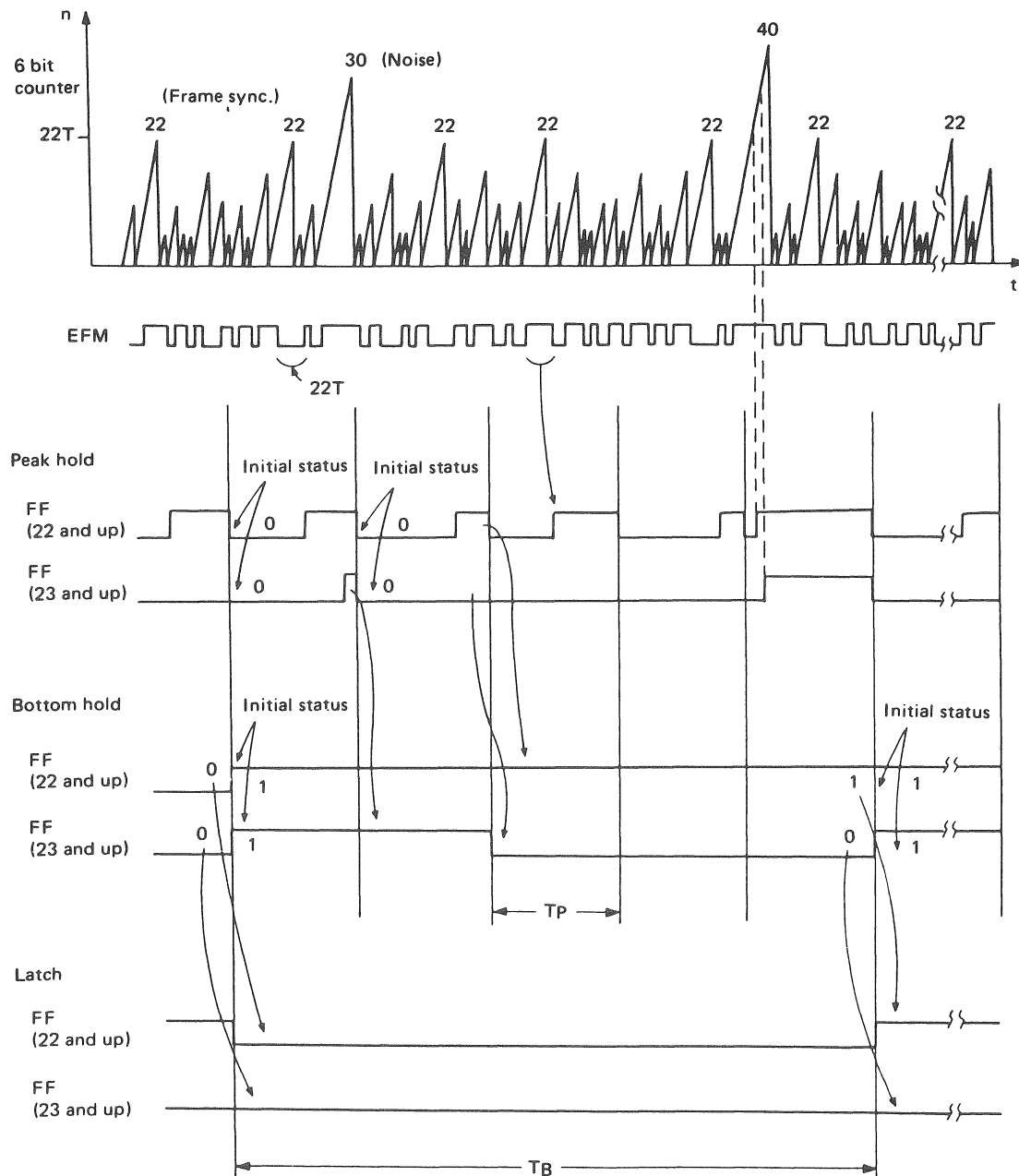


Fig. 3-32 Timing chart in CLV-S, CLV-H mode (2)

7) CLV-A : Register E = 0110'B

Mode used during usual play.

Samples GFS signal ("H" when locked; "L" when unlocked) from the frame sync. detection, protection and interpolation block by WFCK/16, and operates in CLV-P mode in the case of "H". In the case where "L" level is continued for eight times, switching is made to CLV-S mode automatically. Period setting of peak hold in CLV-S mode, bottom hold period sett-

ing and gain setting in CLV-S, CLV-H mode and setting of the frequency dividing ratio in CLV-P mode are made by register D, and mode selection is made by register E. The details of these registers will be explained in the section of CPU interface.

Note : Output is made out of DA07 terminal when PSSL = "L" with WFCK/4 or WFCK/8 as FCKV, and output is made out of DA08 terminal with RFCK/4 or RFCK/8 as FCKX.

3. DESCRIPTION OF ACTUAL CIRCUIT

3-6 Microcomputer

3-6-1 Terminal connection diagram

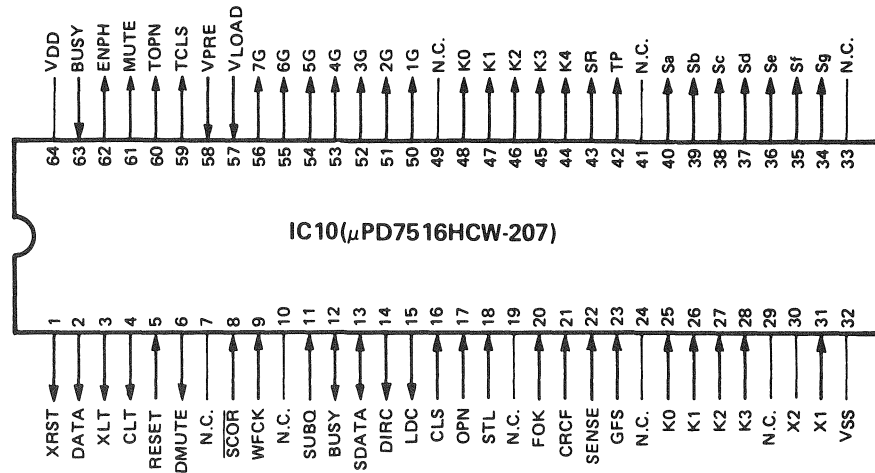


Fig. 3-33

3-6-2 Block diagram

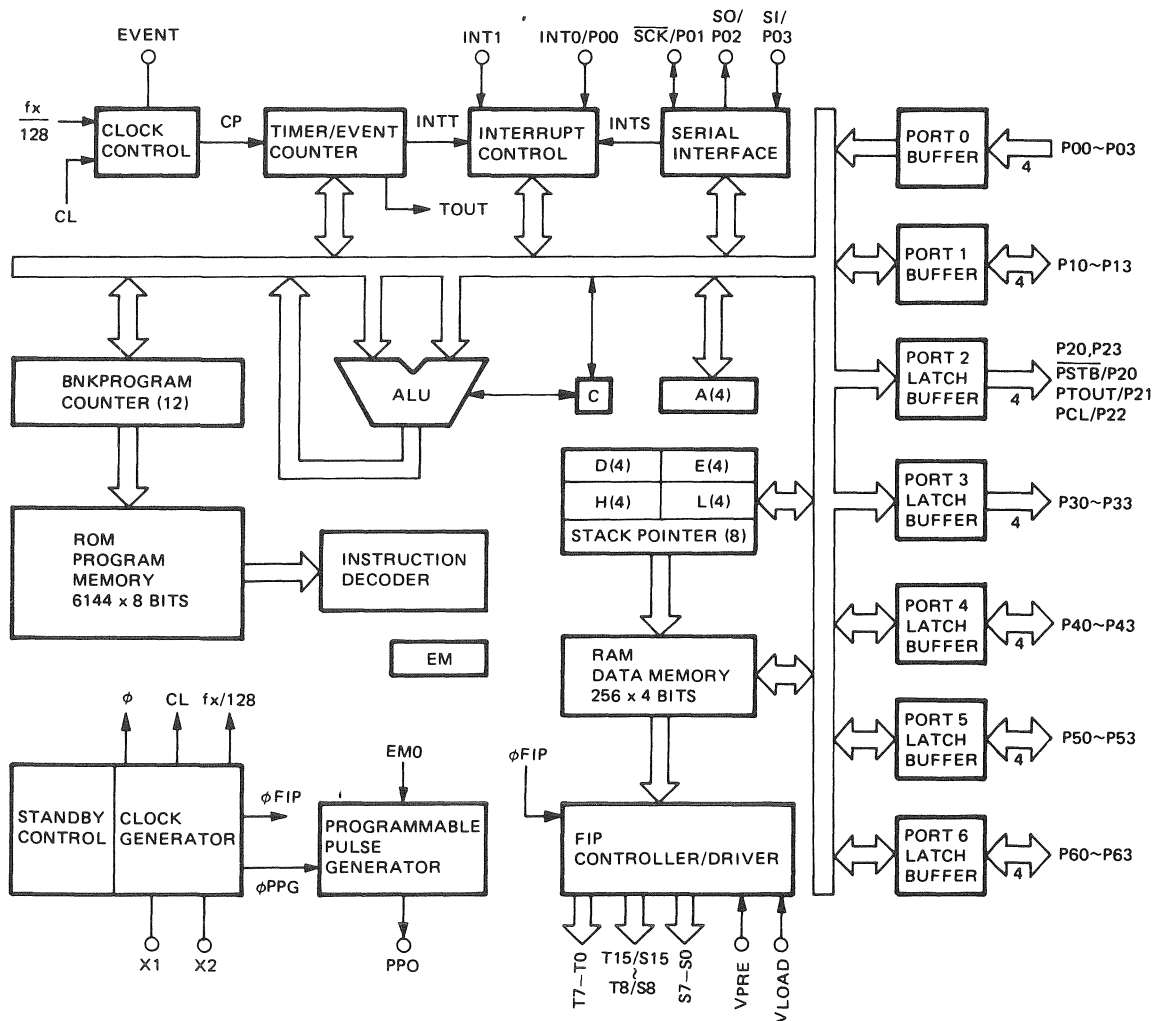


Fig. 3-34

3. DESCRIPTION OF ACTUAL CIRCUIT

3-6-3 Explanation of terminals

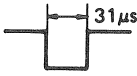
Terminal No.	Name	I/O	Explanation
1	XRST	O	RESET of CX23035 and CX20108 
2	DATA	O	Control data signal to CX23035 and CX20108
3	XLT	O	Control data latch signal to CX23035 and CX20108
4	CLT	O	Control data clock signal to CX23035 and CX20108
5	RESET	I	RESET signal
6	D MUTE	O	Digital muting signal
8	SCOR	I	Q data synchronizing signal interruption
9	WFCK	I	Q data clock signal
11	SUBQ	I	Q data signal
12	BUSY	I/O	Synchronizing BUSY signal
13	S DATA	I/O	Synchronizing DATA signal
14	DIRC	O	Control signal to CX20108 (used at the time of tracking kick)
15	LDC	O	Laser POWER ON signal ("L" : Laser ON)
16	CLS	I	Tray CLOSE signal ("L" : Tray CLOSE)
17	OPN	I	Tray OPEN signal ("L" : Tray OPEN)
18	STL	I	PU's innermost position detect signal ("L" : Innermost position)
20	FOK	I	Focus OK signal ("H" : Focus OK)
21	CRCF	I	Q data CRC OK signal ("H" : CRC OK)
22	SENSE	I	SENSE signal from CX23035 and CX20108.
23	GFS	I	EFM synchronizing OK signal from CX23035. When GFS : "H" occurs in the tracking servo ON status, it indicates that EFM is normally read with CX23035.
25~28	K0~K3	I	Key data signal
30	X2		Clock oscillation crystal connect terminal (oscillation frequency 6.144MHz)
31	X1		
32	Vss		GND
34~40	Sg~Sa	O	Fluorescent display tube segment signal
42	TP	O	Test mode start signal
43	SR	O	Synchronizing signal for X-3WS (Cassette tape deck)
44~48	K4~K0	O	Key matrix signal
50~56	1G~7G	O	Fluorescent display tube grid signal
57	VLOAD		Power supply for fluorescent display tube (−30V)
58	VPRE		Power supply for fluorescent display tube (−5V)
59	TCLS	O	Tray CLOSE signal
60	TOPN	O	Tray OPEN signal
61	MUTE	O	Muting signal
62	ENPH	O	Emphasis signal
63	BUSY	I	Synchronizing BUSY signal
64	VDD		Power supply (+ 5V)

Table 3-8

3. DESCRIPTION OF ACTUAL CIRCUIT

3-6-4 NORMAL MODE

● From loading of Q data to display

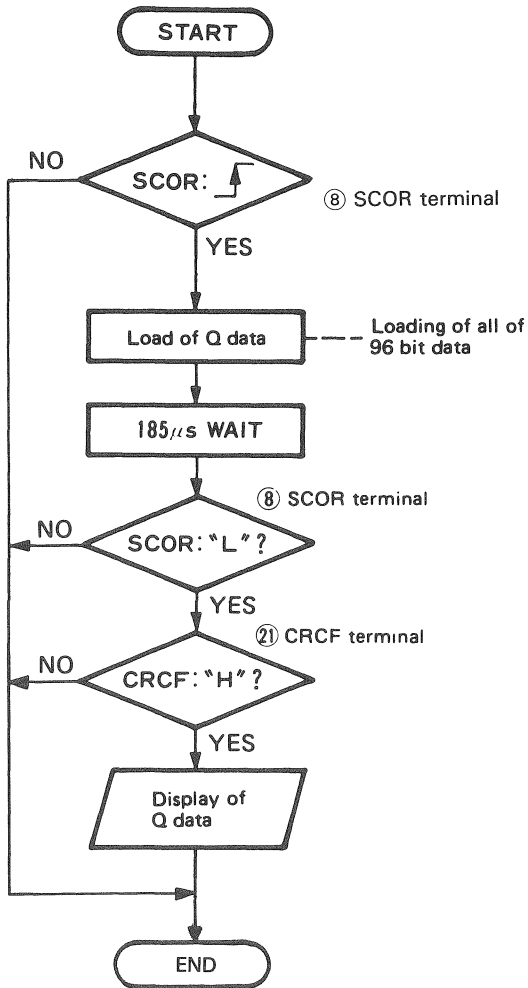


Fig. 3-35

3-6-5 Disk loading to T.O.C. READ

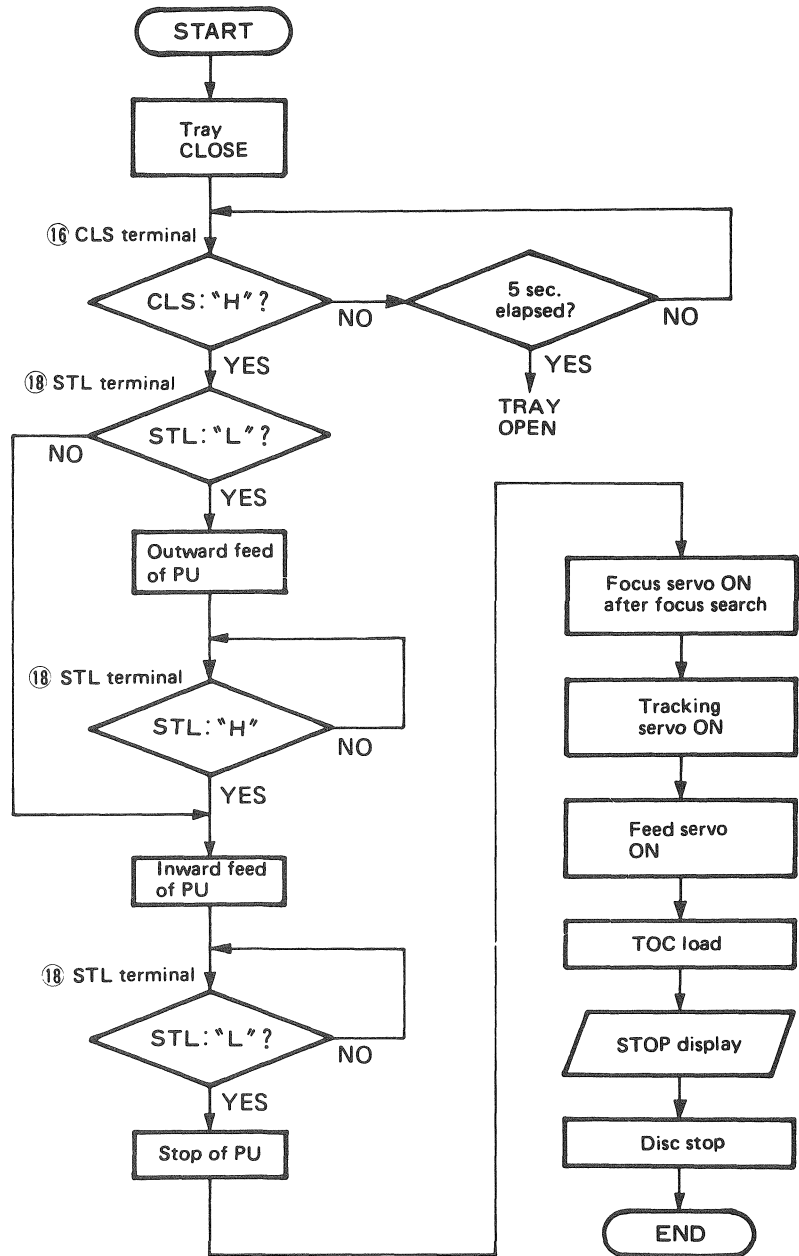


Fig. 3-36

4. TEST MODE

4-1 TEST MODE

The mode the set enters when power is turned on varies depending on the setup of TP20 and TP21. When they are open, the set enters the normal play mode and, when they are short-circuited, it enters the test mode. The relationship of the operation keys and functions in the test mode is shown in Table 4-1.

Each operation including the track jumping (kick) and servo ON-OFF can be controlled separately in the test mode. Allowing the checking of only the focusing servo, for example, the test mode is useful for your troubleshooting operations.

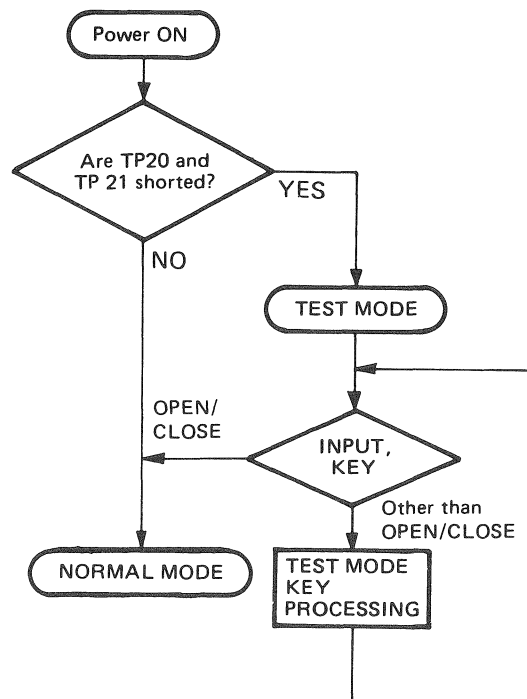


Fig. 4-1

4-2 Explanation of keys during test mode

● Test mode

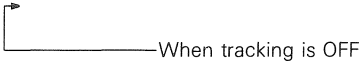
During TEST mode. If you want to try (PUSH THIS KEY)	Function																																												
OPEN/CLOSE	To OPEN/CLOSE the tray. EXIT the Test mode and perform the Normal mode.																																												
Kick (0 ~ 9)	To kick the following number of tracks. Only when Feed is ON (when M-PLAY is lights) (To M-PLAY push PLAY/PAUSE) <table><tr><td>Key No.</td><td>0</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td></tr><tr><td>Direction</td><td colspan="5">FB</td><td colspan="5">FF</td></tr><tr><td>Number of tracks</td><td>512</td><td>64</td><td>16</td><td>3</td><td>1</td><td>1</td><td>3</td><td>16</td><td>64</td><td>512</td></tr><tr><td>Time</td><td>1M</td><td>8s</td><td>2s</td><td>0s</td><td>0s</td><td>0s</td><td>0.5s</td><td>2s</td><td>8s</td><td>1M</td></tr></table> Note : The indicated time is the absolute time change when kick is made. (Time at internal periphery).	Key No.	0	1	2	3	4	5	6	7	8	9	Direction	FB					FF					Number of tracks	512	64	16	3	1	1	3	16	64	512	Time	1M	8s	2s	0s	0s	0s	0.5s	2s	8s	1M
Key No.	0	1	2	3	4	5	6	7	8	9																																			
Direction	FB					FF																																							
Number of tracks	512	64	16	3	1	1	3	16	64	512																																			
Time	1M	8s	2s	0s	0s	0s	0.5s	2s	8s	1M																																			
TRACKING ON (MEMORY)	To turn ON Focus and Tracking. (Feed OFF). Execution is made in the following sequence when focus is OFF. ◦ Focus search → Focus ON → Tracking ON																																												
FOCUS ON (M-READ)	To turn ON Focus. (Tracking, Feed OFF) Execution is made in the following sequence when focus is OFF. ◦ Focus search → Focus ON																																												
STOP (STOP)	To turn OFF Focus, Tracking and Feed. In the case of focus ON (FOK : "H"); focus, tracking and feed are OFF after the disc has stopped. In the case of focus OFF (FOK : "L"), the disc motor is set for free run and focus, tracking and feed are OFF.																																												
Feed ON (PLAY/PAUSE)	To turn ON Focus, Tracking and Feed. Execution is made in the following sequence if focus is OFF and tracking is OFF. ◦ Focus search → Focus ON → Tracking ON → Feed ON 																																												
KICK-OUT (UP)	To move in FWD direction for 100ms, at the time of STOP. To kick 3 tracks in FWD direction when feed is ON.																																												
KICK-IN (DOWN)	To move in BACK direction for 100ms, at the time of STOP. To kick 3 tracks in BACK direction when feed is ON.																																												

Table 4-1

4. TEST MODE

4-3 FLOW CHART FROM TRAY OPEN STATUS AFTER POWER ON

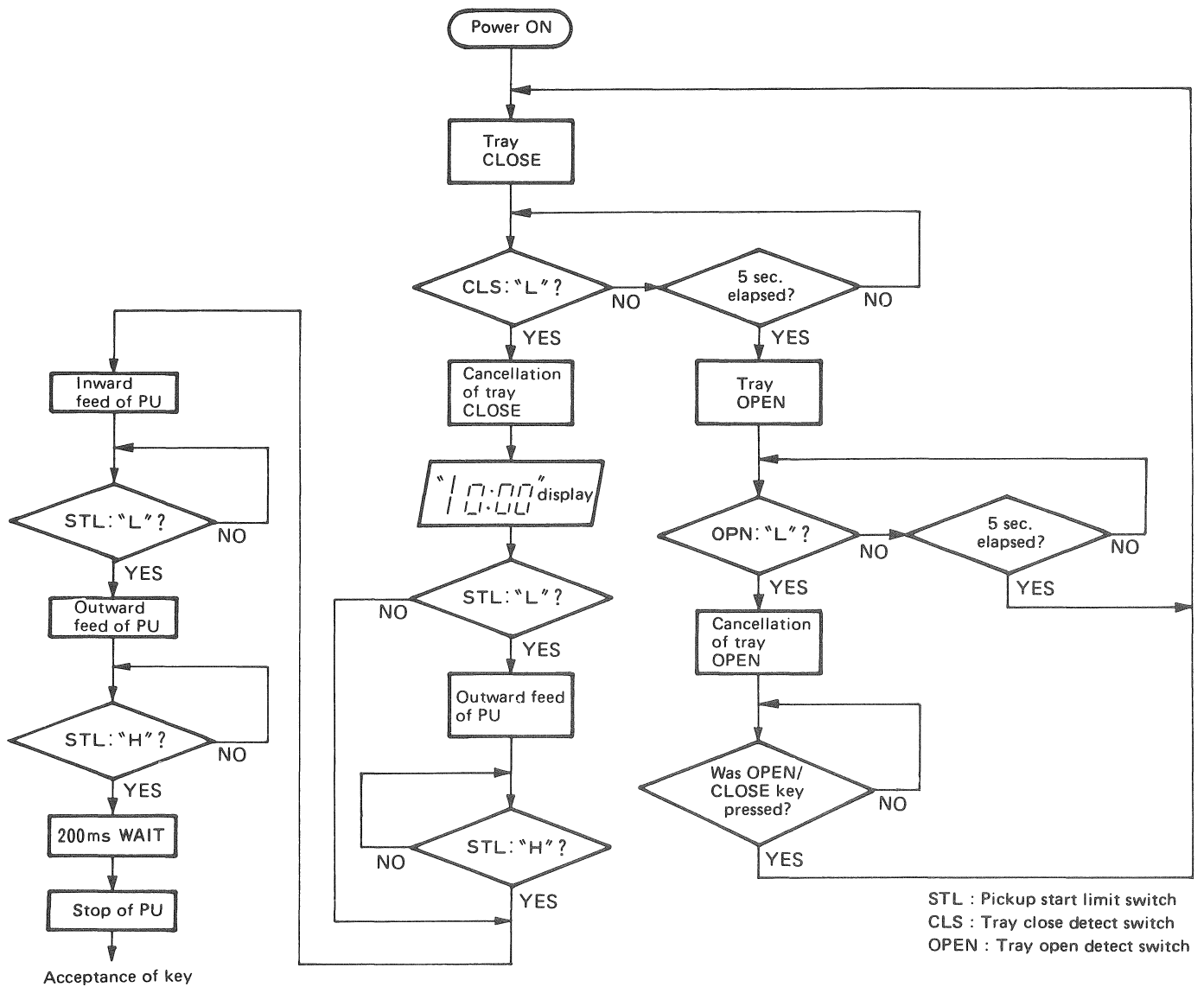


Fig. 4-2

4. TEST MODE

4-4 FOCUS SEARCH & FOCUS SERVO ON

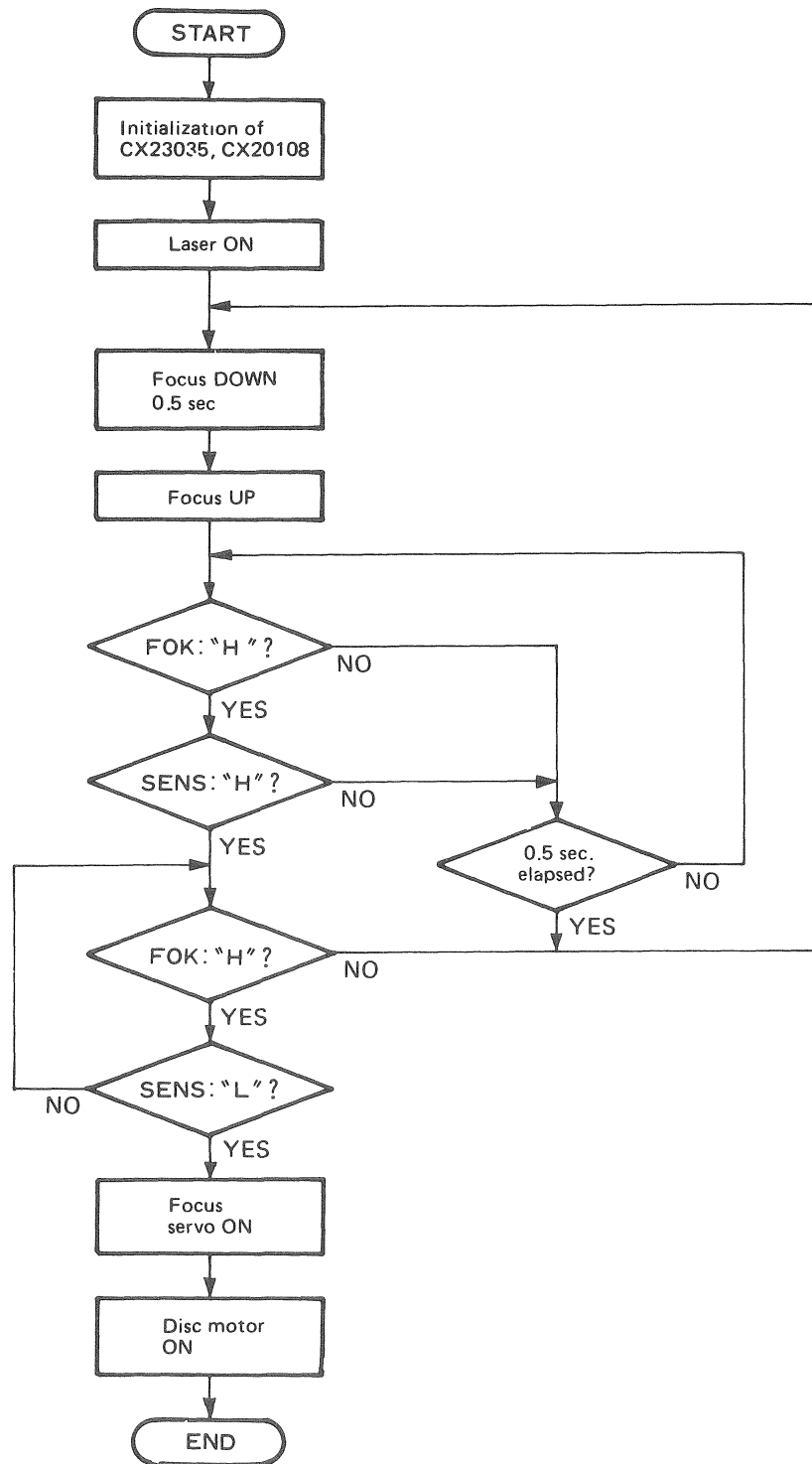


Fig. 4-3

4. TEST MODE

4-5 TRACKING SERVO ON

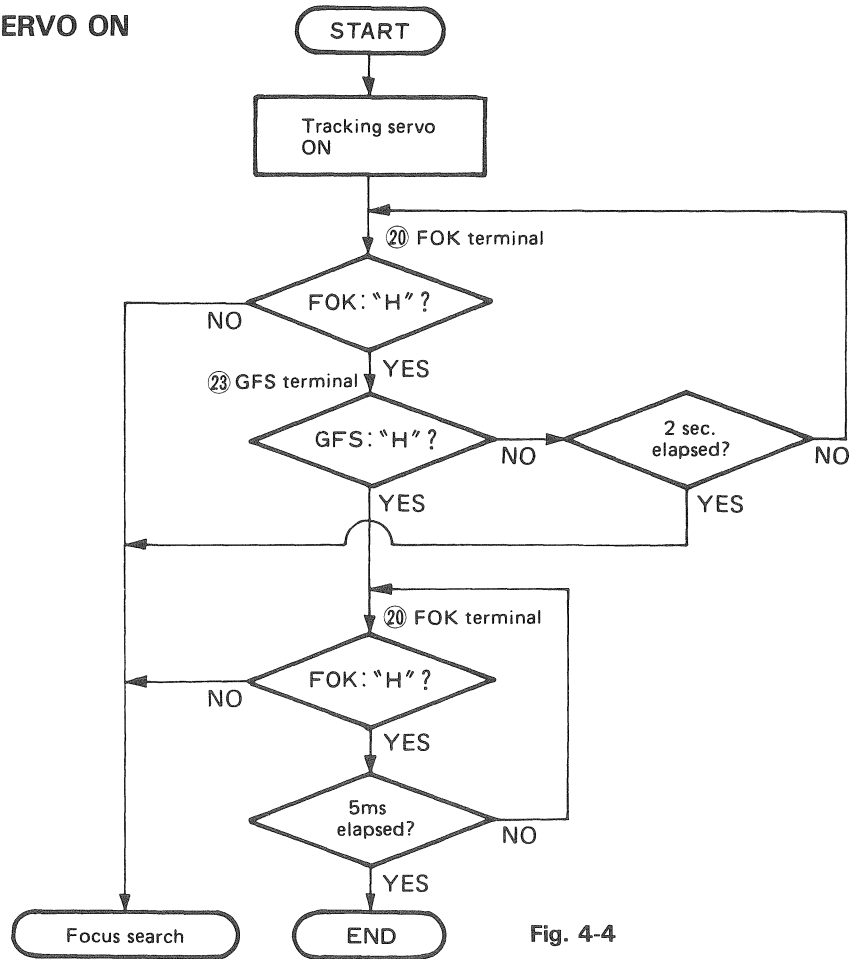


Fig. 4-4

4-6 DISC MOTOR STOP

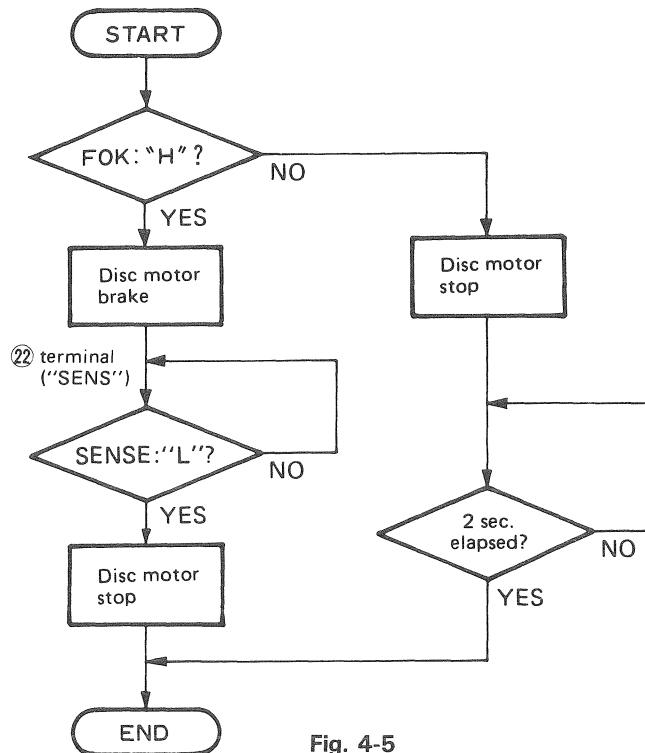


Fig. 4-5

5. TROUBLE SHOOTING

5-1 TOC CANNOT BE READ

(The disc is ejected or the disc cannot be played.)

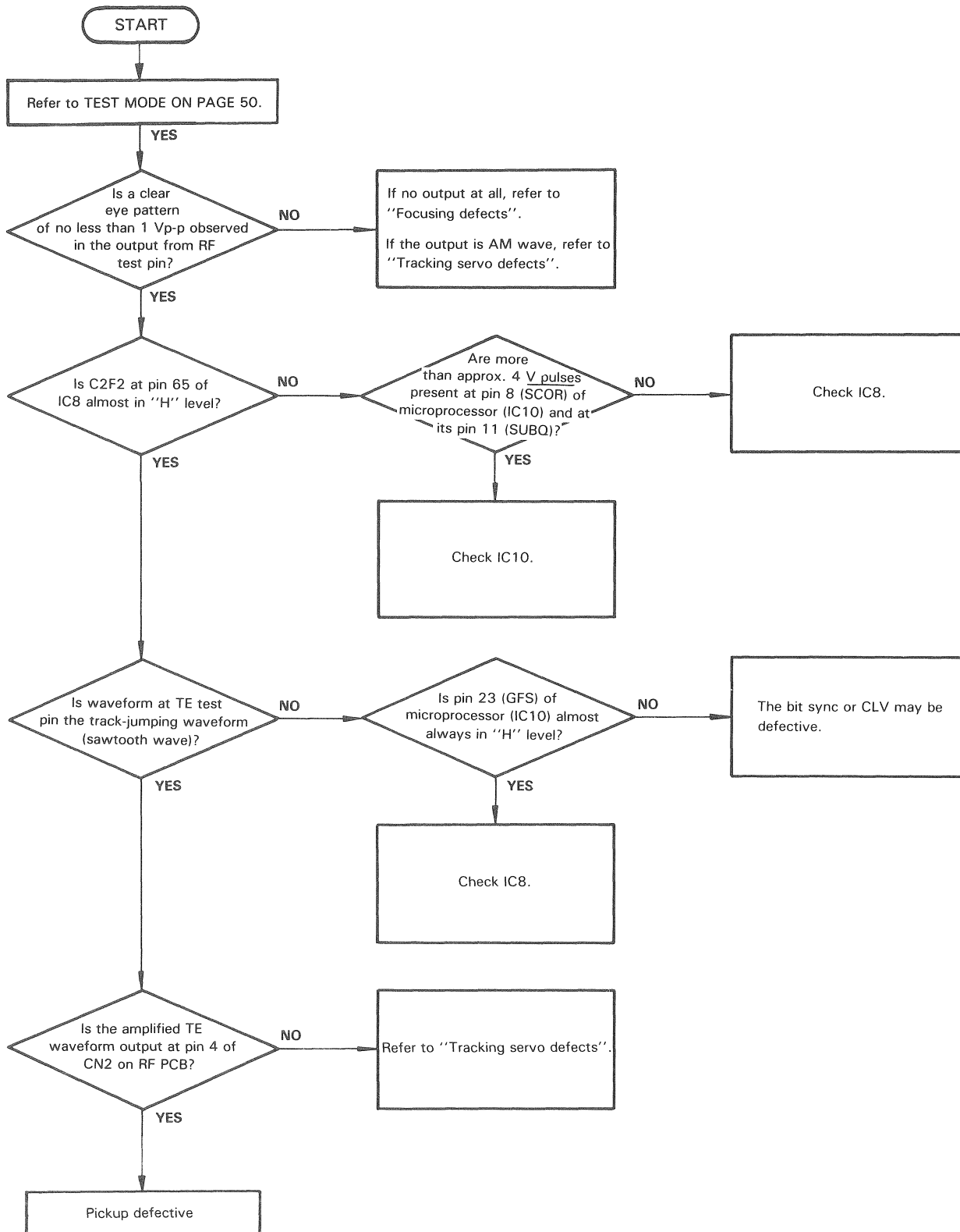


Fig. 5-1

5. TROUBLE SHOOTING

5-2 FOCUSING DEFECTS

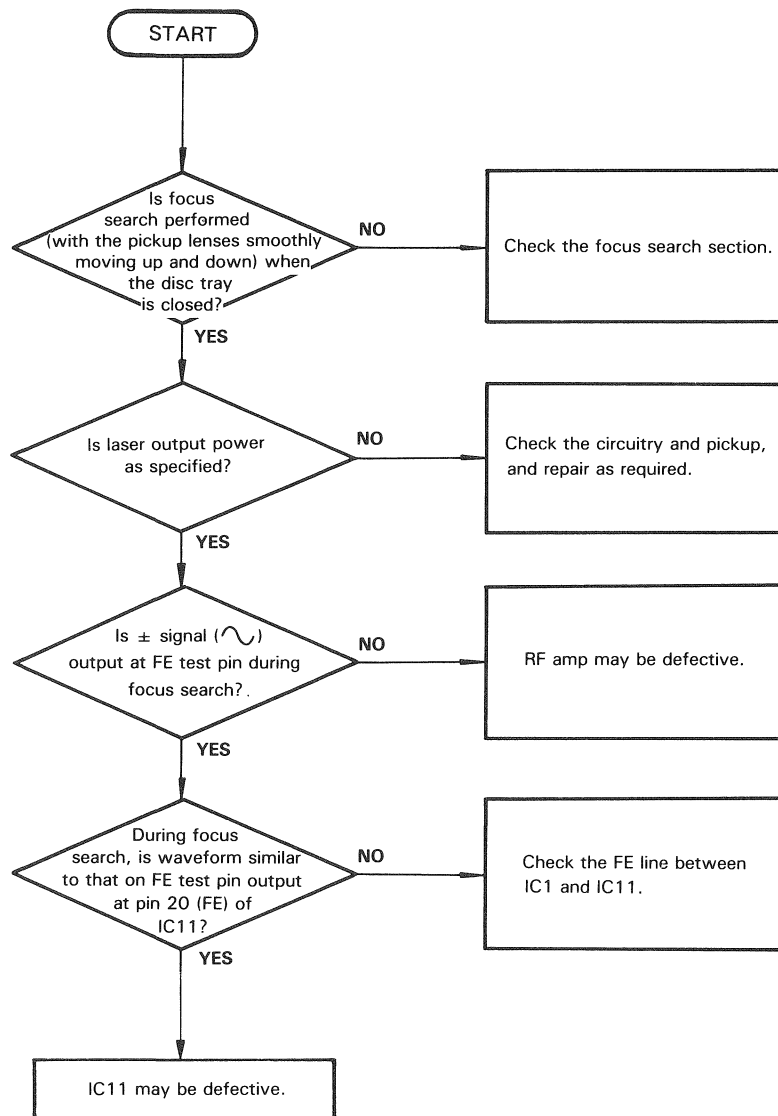


Fig. 5-2

5. TROUBLE SHOOTING

5-3 TRACKING SERVO DEFECTS

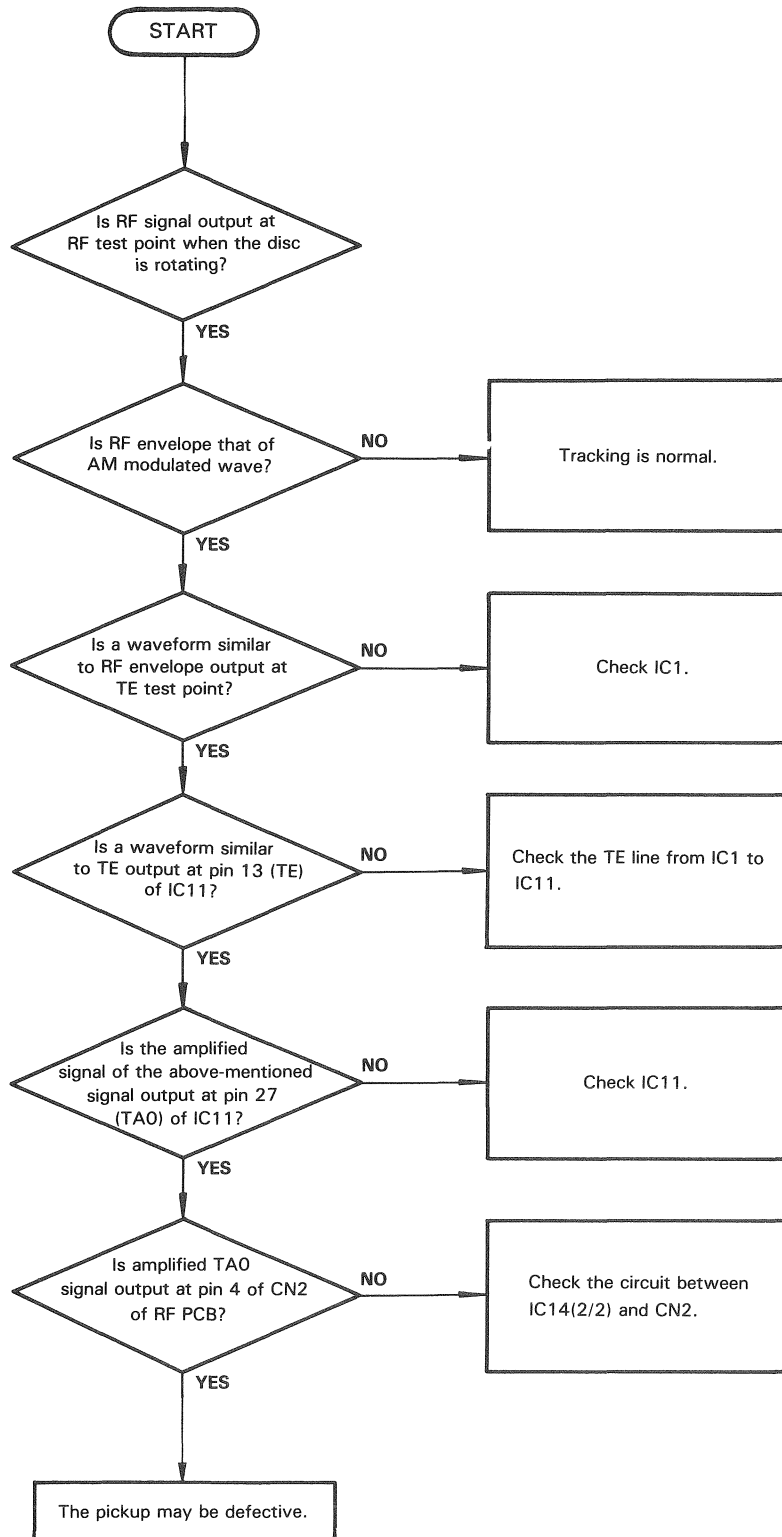


Fig. 5-3

5. TROUBLE SHOOTING

5-4 RF EYE PATTERN

As the clearness varies depending on each model, observe well the pattern on a normal set.

When the pattern is improper, perform radial and tangential adjustment if the pickup has such adjustment SCREWS.

In other cases, the pickup defect is very probable.

The RF may be subject to malfunction if the beginning of the 3T and 4T waveforms are dropping.

5-5 BIT SYNC (WHETHER PLCK IS IN SYNCHRONISM WITH EFM)

Apply PLCK to CH1 input of an oscilloscope, RF (eye pattern) to CH2 and trigger using PLCK. The CH2 RF signal can be observed (stabilized without moving horizontally) if bit sync is OK. If it is not synchronized, observation is impossible due to the horizontal flow of waveforms.

In this case, there may be misadjustment in VCO or a part may be defective.

5-6 FRAME SYNC

Frame sync is OK if the sync signal for the EFM signal can be confirmed with the EFM decoder. It can be checked by the "H" level of pin GFS of the signal processor IC.

5-7 DATA ERROR RATE

When the signal processor IC is CX23035, the Q data error rate can be checked with the output at pin CRCF. (L when erroneous)

When the IC is TC9179F, the EFM data error rate of a DP-1100 series unit is output at pin 1 of SVC microprocessor IC12. The error rate is normal when the level is "L" during playing and the number of "H" pulses observed on the oscilloscope screen is no more than 5.

As stains or scratches on the disc are also counted as an error, use a specified, high-quality disc for checking.

5-8 CLV SERVO

Signal names inside () are those of CX23035.

When the disc motor is started, AFC0 (MDS) goes "H" to drive the motor at maximum power.

During playing, the CLV servo is locked correctly if both AFC0 (MDS) and APC0 (MDP) output voltages at 50% average values.

Be careful in this judgement because the above-mentioned waveforms also vary when the disc motor itself is defective.

6. CHECK OF PICK-UP

DP-770 PICKUP OPERATION DEFECTIVE PARTS CHECK FLOW

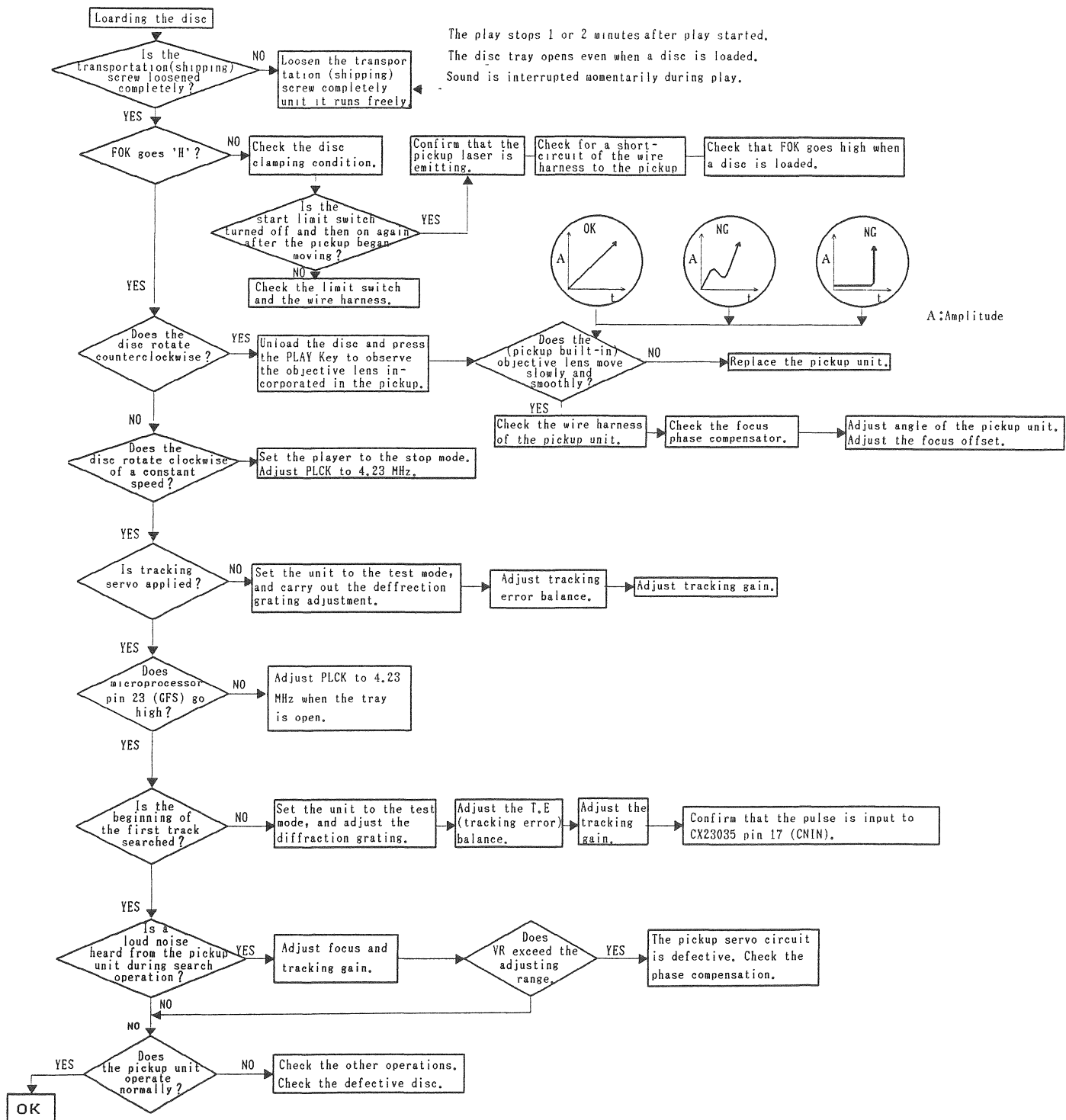
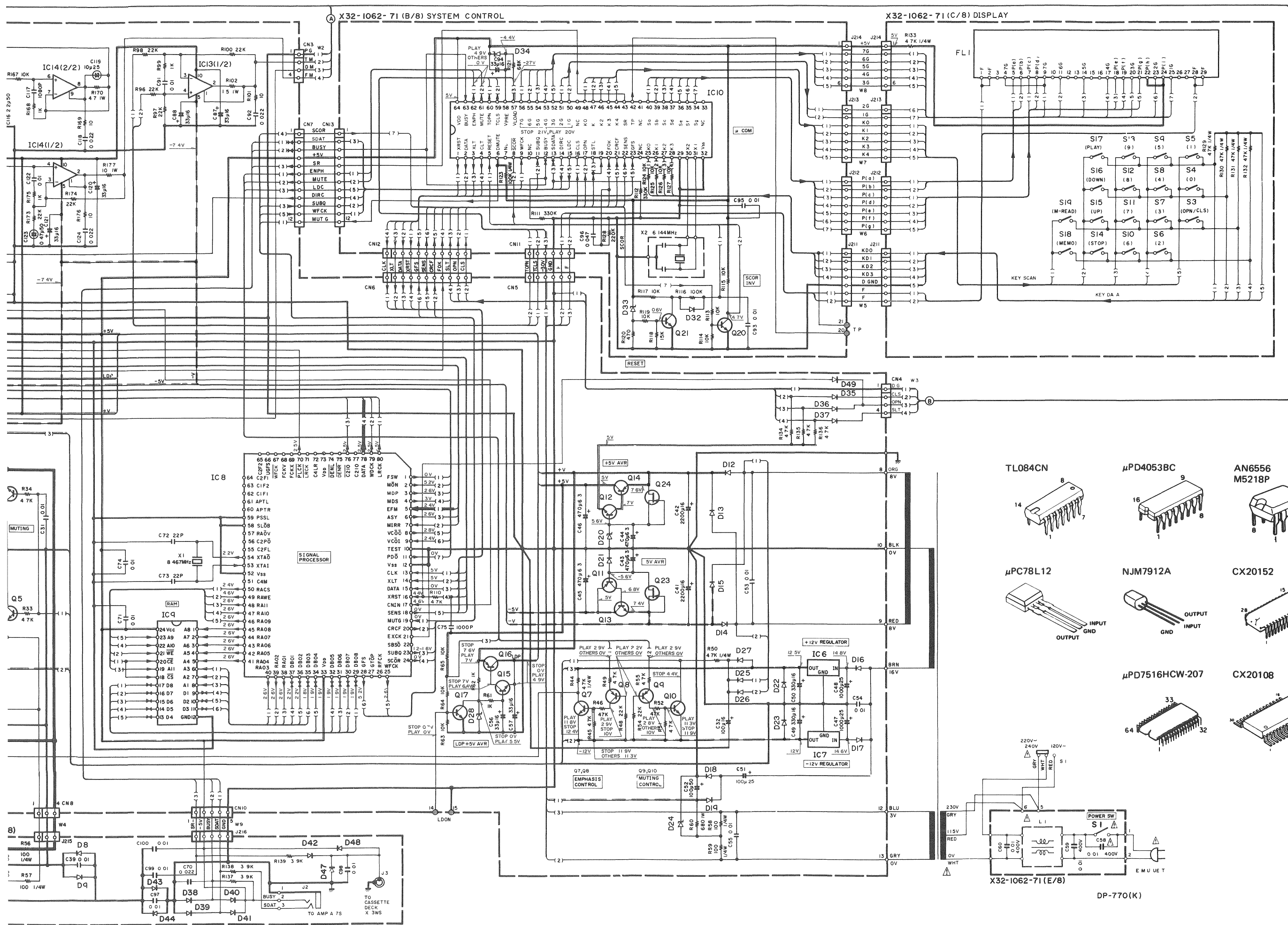
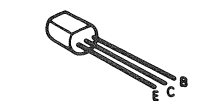


Fig. 6-1



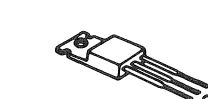
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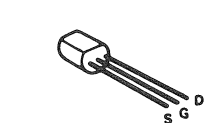
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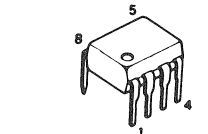
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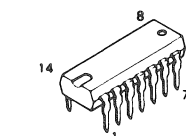
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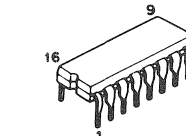
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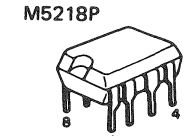
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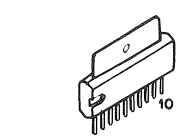
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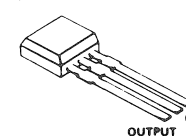
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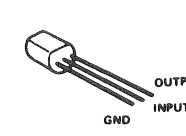
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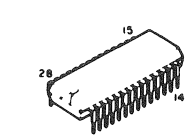
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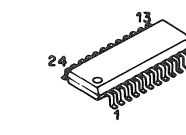
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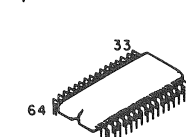
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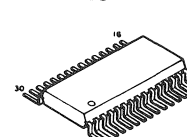
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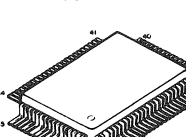
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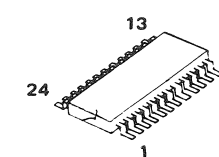
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CX23035



HM6116FP-4



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