Ordering number : EN4340A

Thick Film Hybrid IC

STK400-050

AF Power Amplifier (Split Power Supply) (30 W + 30 W + 30 W min, THD = 0.4%)

Overview

Now, thick-film audio power amplifier ICs are available with pin-compatibility to permit a single PCB to be designed and amplifier output capacity changed simply by installing a hybrid IC. This new series was developed with this kind of pin-compatibility to ensure integration between systems everywhere. With this new series of IC, even changes from 3-channel amplifier to 2-channel amplifiers is possible using the same PCB. In addition, this new series of ICs has a 6/3Ω drive in order to support the low impedance of modern speakers.

Features

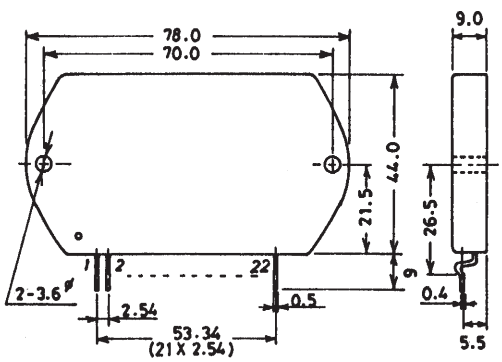
- Pin-compatible
  STK400-000 series (3-channel, single package)
  ↓
  STK401-000 series (2-channel, single package)
- Output load impedance RL=6Ω/3Ω supported
- New pin arrangement
  To simplify input/output pattern layout and minimize the effects of pattern layout on operational characteristics, pin assignments are grouped into blocks consisting of input, output and power systems.
- Few external circuits
  Compared to those series used until now, capacitors and boot-strap resistors for external circuits can be greatly reduced.

Package Dimensions

unit: mm

4086A

[STK400-050]



Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		±39	V
Thermal resistance	θj-c	Per power transistor	1.8	°C/W
Junction temperature	Tj		150	°C
Operating substrate temperature	Tc		125	°C
Storage temperature range	Tstg		–30 to +125	°C
Available time for load short-circuit	t_s	V_{CC} = ±26 V, R_L = 6 Ω, f = 50 Hz, P_O = 30 W	1	s

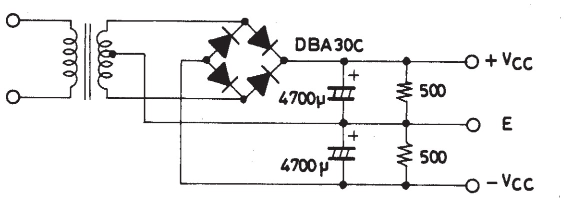
Operating Characteristics at Ta = 25°C, R_L = 6Ω, Rg = 600Ω, VG = 40dB, R_L (non-inductive)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current	I_{CCO}	V_{CC} =± 31 V	30	90	150	mA
Output power	P_O (1)	V_{CC} = ±26 V, f = 20 Hz to 20 kHz, THD = 0.4%	30	35		W
	P_O (2)	V_{CC} = ±22 V, f = 1 kHz, THD = 1.0%, R_L = 3 Ω	30	35		W
Total harmonic distortion	THD (1)	V_{CC} = ±26 V, f = 20 Hz to 20 kHz, P_O = 1.0 W			0.4	%
	THD (2)	V_{CC} = ±26 V, f = 1 kHz, P_O = 5.0 W		0.01		%
Frequency response	f_L, f_H	V_{CC} = ±26 V, P_O = 1.0 W, $^{+0}_{-3}$ dB		20 to 50 k		Hz
Input impedance	r_i	V_{CC} = ±26 V, f = 1 kHz, P_O = 1.0 W		55		kΩ
Output noise voltage	V_{NO}	V_{CC} = ±31 V, Rg = 10 kΩ			1.2	mVrms
Neutral voltage	V_N	V_{CC} = ±31 V	–70	0	+70	mV

Notes

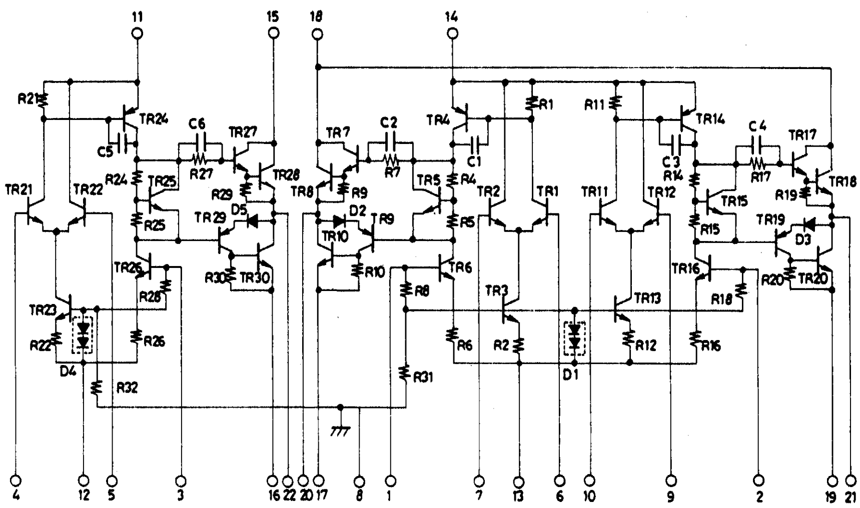
- Use rated power supply for test unless otherwise specified.
- When measuring available time for load short-circuit and output noise voltage use transformer power supply indicated below.
- Output noise voltage is represented by the peak value rms (VTVM) for mean reading. Use an AC stabilized power supply (50 Hz) on the primary side to eliminate the effect of AC flicker noise.

Specified Transformer Power Supply (RP-25 Equivalent)

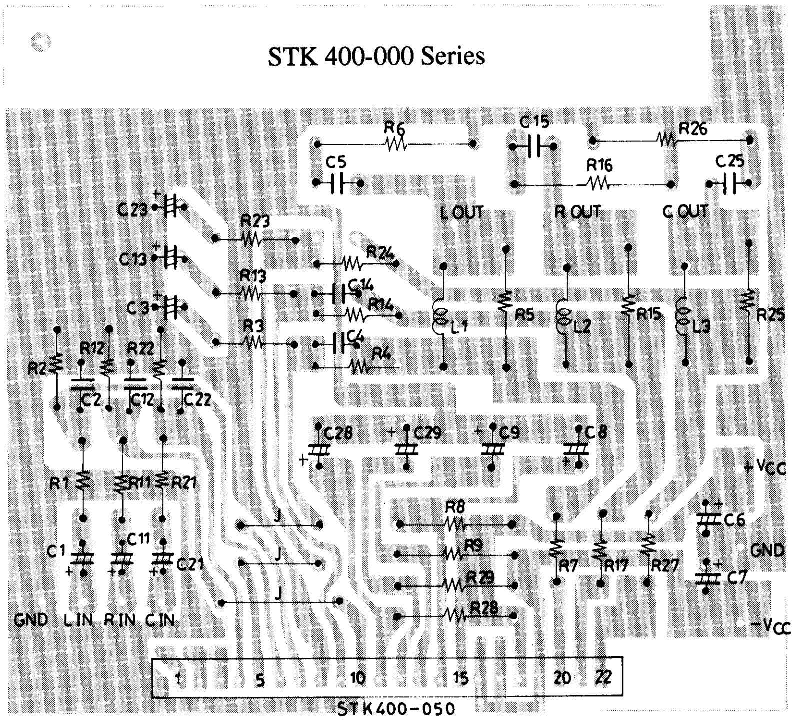


Unit (resistance:Ω, capacitance:F)

Internal Equivalent Circuit



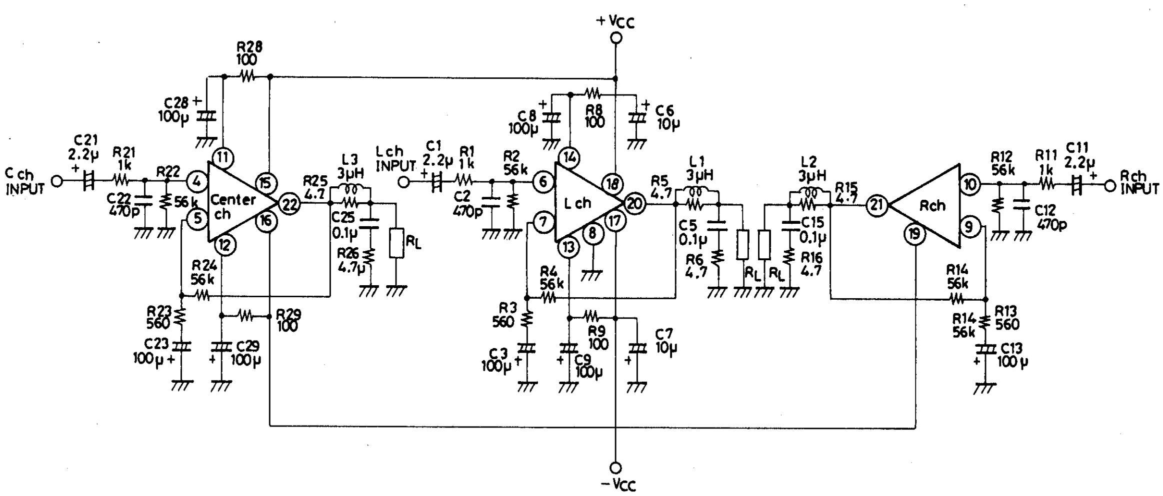
Pattern Example for PCB used with either 2- or 3-channel Amplifiers.



Copper (Cu) foil surface

In the STK401-000 series, pin No. 6 corresponds to pin No. 1.

Sample Application Circuit



Unit (resistance:Ω, capacitance:F)

Description of External Circuits

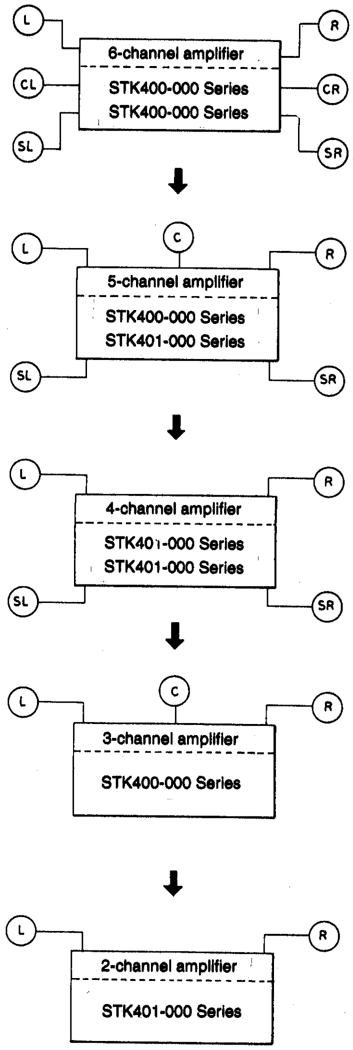
C1, 11, 21	For input coupling capacitor. Used for current blocking. When capacitor reactance with low frequency is increased, the reactance value should be reduced in order to reduce the output noise from the signal resistance dependent 1/f noise. In response to the popping noise which occurs when the system power is turned on, C1 and C11 which determine the decay time constant on the input side are increased while C3, C13 and C23 on the NF side are decreased.
C2, 12, 22	For input filter capacitor. Permits high-region noise reduction by utilizing filter constructed with R1, R11 and R21.
C3, 13, 23	For NF capacitor. This capacitor determines the decline of the cut-off frequency and is calculated according to the following equation. $f_L = \dfrac{1}{2\pi \text{ X C3 (13, 23,) X R3 (13, 23)}}$ For the purpose of achieving voltage gains prior to reduction, it is best that C3, C13 and C23 are large. However, because the shock noise which occurs when the system power is turned on tends to increase, values larger than those absolutely necessary should be avoided.
C5, 15, 25	For oscillation prevention capacitor. A Mylar capacitor with temperature and frequency features is recommended.
C6, 7	For oscillation prevention capacitor. To ensure safe IC functioning, the capacitor should be installed as close as possible to the IC power pin to reduce power impedance. An electrolytic capacitor is good.
C8, 9, 28, 29	For decoupling capacitor. Reduces shock noise during power up using decay time constant circuits with R8, R9, R28 and R29 and eliminates components such as ripples crossing over into the input side from the power line.
R1, 11, 21	For input filter applied resistor.
R2, 12, 22	For input bias resistor. The input pin is biased to zero potential. Input impedance is mostly decided with this resistance value.
R3, 13, 23 R4, 14, 24	For resistors to determine voltage gain (VG). We recommend a VG = 40 dB using R3, R13, R23 = 560Ω and R4, R14 and R24 = 56Ω. VG adjustments are best performed using R3, R13 and R23. When using R4, R14 and R24 for such purposes, R4, R14 and R24 should be set to equal R2, R12 and R22 in order to establish a stable VN balance.
R5, 15, 25	For oscillation prevention resistor.
R6, 16, 26	For oscillation prevention resistor. This resistor's electrical output resides in the signal frequency and is calculated according to the following formula. $P\ R6\ (16, 26) = \left(\dfrac{V_{CC}\ max/\sqrt{2}}{1/2\pi\ fC5\ (15, 25) + R6\ (16, 26)}\right)^2 \text{ X R6 (16, 26)}$ f = output signal frequency upper limit
R8, 9, 28, 29	For ripple filter applied resistor. PO max, ripple rejection and power-up shock noise are modified according to this value. Set the electrical output of these resistors while keeping in mind the flow of peak current during recharging to C8, C9, C28 and C29 which function as pre-drive TR control resistors during load shorts.
L1, 2, 3	For oscillation prevention coil. Compensates phase dislocation caused by load capacitors and ensures stable oscillation.

Series Configuration

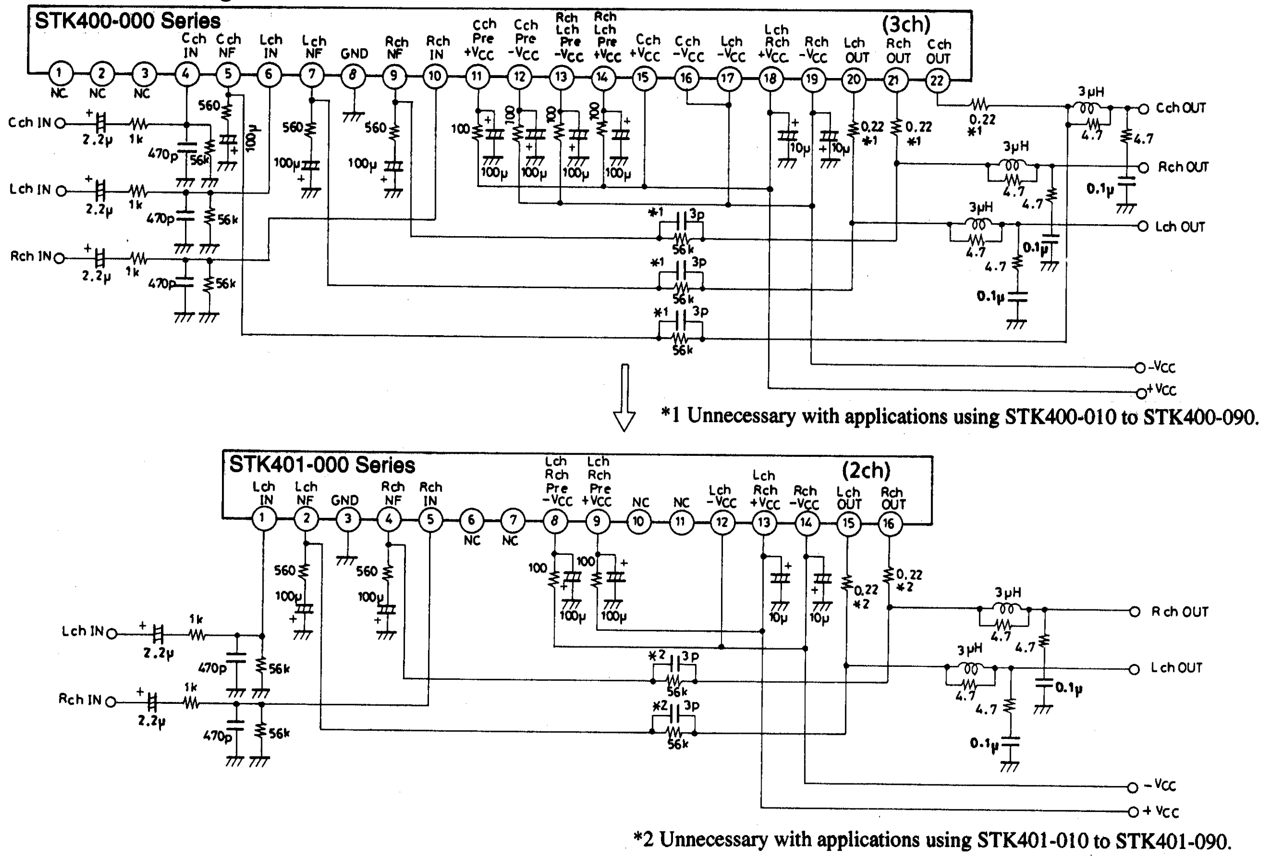
3ch Amp IC Name	Fixed Standard Output	2ch Amp IC Name	Fixed Standard Output	THD [%] f = 20 to 20kHz	Supply voltage			
					V_{CC} max1	V_{CC} max2	$V_{CC}1$	$V_{CC}2$
STK400-010	10W X 3	STK401-010	10W X 2	0.4	—	±27	±18	±14
STK400-020	15W X 3	STK401-020	15W X 2		—	±29	±20	±16
STK400-030	20W X 3	STK401-030	20W X 2		—	±34	±23	±19
STK400-040	25W X 3	STK401-040	25W X 2		—	±36	±25	±21
STK400-050	30W X 3	STK401-050	30W X 2		—	±39	±26	±22
STK400-060	35W X 3	STK401-060	35W X 2		—	±41	±28	±23
STK400-070	40W X 3	STK401-070	40W X 2		—	±44	±30	±24
STK400-080	45W X 3	STK401-080	45W X 2		—	±45	±31	±25
STK400-090	50W X 3	STK401-090	50W X 2		—	±47	±32	±26
STK400-100	60W X 3	STK401-100	60W X 2		—	±51	±35	±27
STK400-110	70W X 3	STK401-110	70W X 2		±56.0	—	±38	—
—	—	STK401-120	80W X 2		±61.0	—	±42	—
—	—	STK401-130	100W X 2		±65.0	—	±45	—
—	—	STK401-140	120W X 2		±74.0	—	±51	—

V_{CC} max1 R_L = 6Ω
V_{CC} max2 R_L = 6Ω to 3Ω operation
$V_{CC}1$ R_L = 6Ω operation
$V_{CC}2$ R_L = 3Ω operation

Example of Set Design for Common PCB



External Circuit Diagram



Unit (resistance:Ω, capacitance:F)

Heat Radiation Design Considerations

The radiator thermal resistance θc-a required for total substrate power dissipation Pd in the STK400-050 is determined as:

Condition 1: IC substrate temperature Tc not to exceed 125°C.

Pd x θc-a+Ta <125°C ························(1)···

where Ta is set assured ambient temperature.

Condition 2: Power transistor junction temperature Tj not to exceed 150°C.

Pd x θc-a+Pd/N x θj-c+Ta<150°C·········(2)

where N is the number of power transistors and θj-c the thermal resistance per power transistor chip. However, power transistor power consumption is Pd equally divided by N units.

Expressions (1) and (2) can be rewritten based on θc-a to yield:

θc-a<(125–Ta)/Pd ···························(1)'·····

θc-a<(150–Ta)/Pd–θj-c/N ···················(2)'··

The required radiator thermal resistance will satisfy both of these expressions.

From expressions (1)' and (2)', the required radiator thermal resistance can be determined once the following specifications are known:

- Supply voltage V_{CC}
- Load resistance R_L
- Assured ambient temperature Ta

The total substrate power consumption when STK400-050 V_{CC} is ±26 V and R_L is 6 Ω, for a continuous sine wave signal, is a maximum of 70W (Fig. 1). In general, when this sort of continuous signal is used for estimation of power consumption, the Pd used is 1/10th of P_O max (slight variation depending on safety standard).

Pd=42.5W (1/10 P_O max=during 3W)

The STK400-050 has six power transistors, so the thermal resistance per transistor θj-c is 1.8°C / W. With an assured ambient temperature Ta of 50°C, the required radiator thermal resistance θc-a would be:

From expression (1)' θc-a <(125–50)/42.5
<1.76
From expression (2)' θc-a <(150–50)/42.5–1.8/6
<2.05

To satisfy both, 1.76°C/W is the required radiator thermal resistance.

Figure 2 illustrates Pd - P_O when the V_{CC} of STK400-050 is ±19V and R_L is functioning at 3Ω.

Pd = 51W (1/10 P_O max = during 3W)
From expression (1)' θc-a <(125–50)-51
<1.47
From expression (2)' θc-a <(150-50)/51-1.8/6
<1.66

To satisfy both, 1.47°C / W is the required radiator thermal resistance. This design example is based on a fixed voltage supply, and will require verification within your specific set environment.

Figure 1

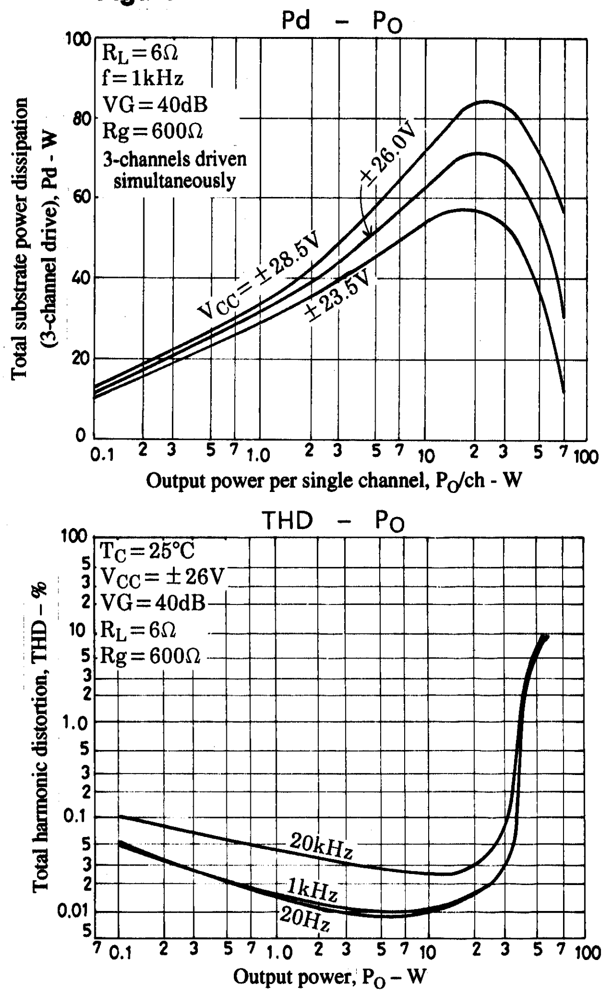
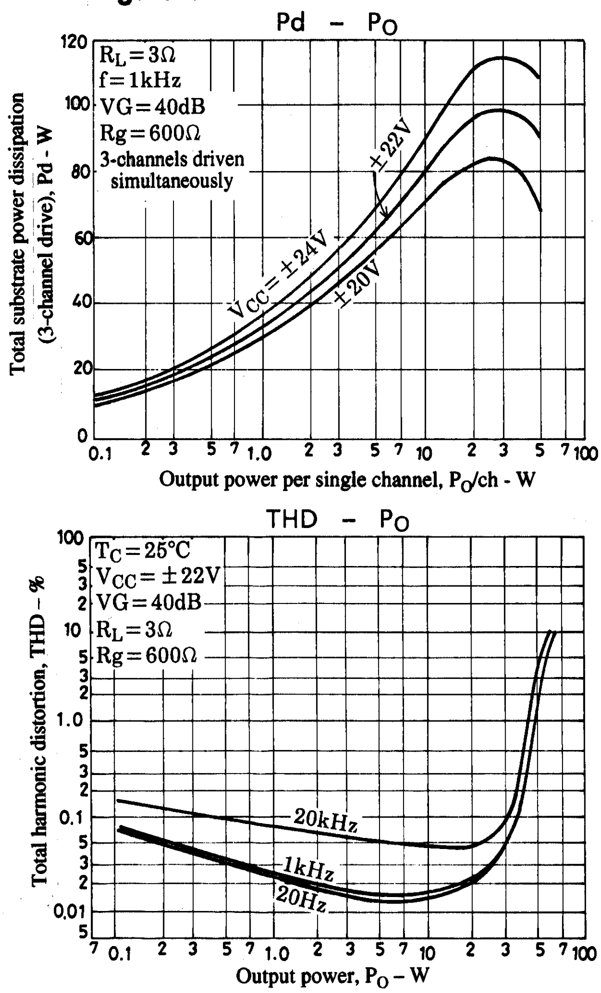
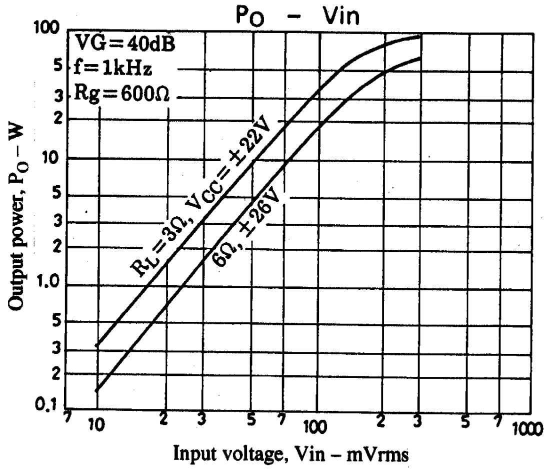
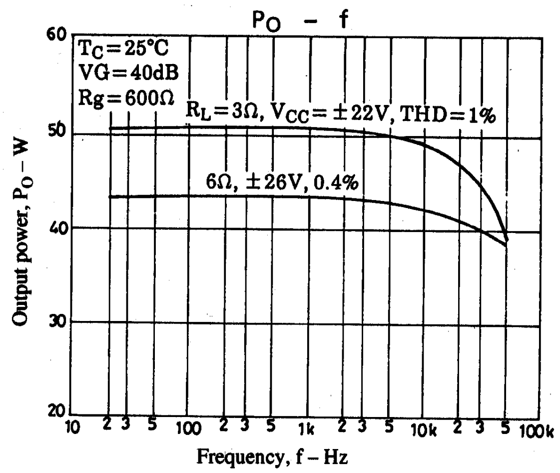
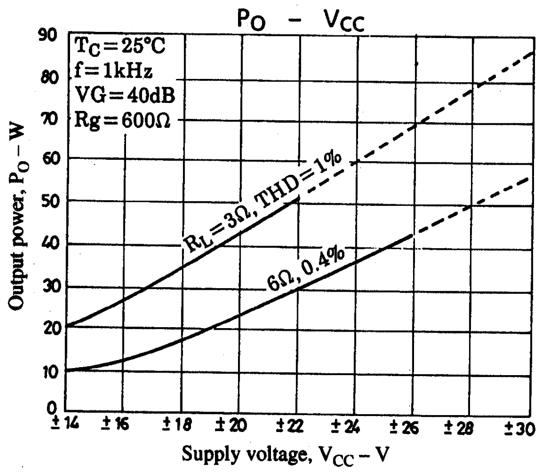


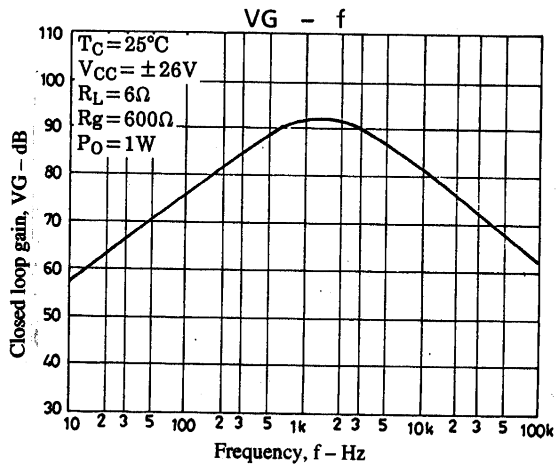
Figure 2

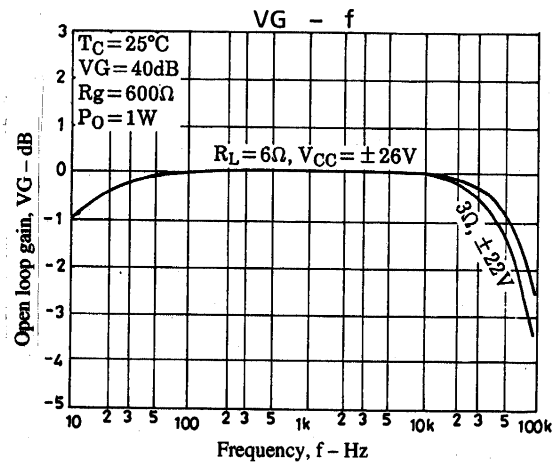


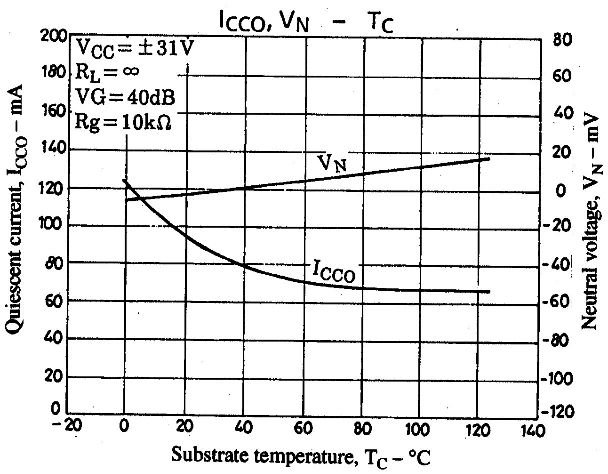

Po - Vin
VG=40dB
f=1kHz
Rg=600Ω
RL=3Ω, VCC=±22V
6Ω, ±26V
Output power, PO – W
Input voltage, Vin – mVrms

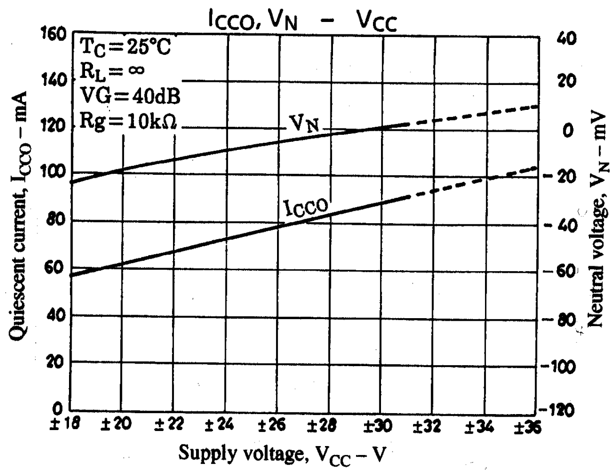

Po - f
TC=25°C
VG=40dB
Rg=600Ω
RL=3Ω, VCC=±22V, THD=1%
6Ω, ±26V, 0.4%
Output power, PO – W
Frequency, f – Hz


Po - Vcc
TC=25°C
f=1kHz
VG=40dB
Rg=600Ω
RL=3Ω, THD=1%
6Ω, 0.4%
Output power, PO – W
Supply voltage, VCC – V


VG - f
TC=25°C
VCC=±26V
RL=6Ω
Rg=600Ω
PO=1W
Closed loop gain, VG – dB
Frequency, f – Hz


VG - f
TC=25°C
VG=40dB
Rg=600Ω
PO=1W
RL=6Ω, VCC=±26V
3Ω, ±22V
Open loop gain, VG – dB
Frequency, f – Hz


ICCO, VN - TC
VCC=±31V
RL=∞
VG=40dB
Rg=10kΩ
VN
ICCO
Quiescent current, ICCO – mA
Neutral voltage, VN – mV
Substrate temperature, TC – °C


ICCO, VN - VCC
TC=25°C
RL=∞
VG=40dB
Rg=10kΩ
VN
ICCO
Quiescent current, ICCO – mA
Neutral voltage, VN – mV
Supply voltage, VCC – V