MN66271RA

Signal Processing LSI for Compact Disc Players

■ Overview

The MN66271RA is a CD signal processing LSI that, on a single chip, combines optics servos for the CD player (focus, tracking, and traverse servos), digital signal processing (EFM demodulation and error correction), digital servo processing for the spindle motor, digital filter, and D/A converter, so thus covers all signal processing functions from the head's RF amplifier onward.

■ Features

(Optics servo)

- Focus, tracking, and traverse servos
- Automatic adjustment functions for FO/TR gain, FO/TR offset, and FO/TR balance
- Built-in D/A converter for drive voltage output
- Built-in dropout countermeasures
- Anti-shock functions
- Built-in track cross counter
- Support for both linear motor and screw-based traverse mechanisms
- Support for 3- and 1-beam systems Digital Signal Processing

(Digital signal processing)

- Built-in DSL and PLL
- Frame synchronization detection, holding, and insertion
- Subcode data processing
  - Subcode Q data CRC check
  - Built-in subcode Q data register
- CIRC error detection and correction
  - C1 decoder: duplex error correction
  - C2 decoder: triplex error correction
  - Built-in 16-K bits of RAM for use in de-interleaving
- Audio data interpolation
  - Averaging or retention of previous values
  - Soft muting
  - Digital attenuation (256 levels)
- Software attenuation (256 levels)
- Audio data peak level detection function
- Automatic cuing detection function
- Digital audio interface (EIAJ format)
- Audio data serial interface

(Spindle motor servo)

- CLV digital servo

(Audio circuits)

- Digital filter using 8 times oversampling
- Built-in D/A converter (1-bit D/A converter)
- Built-in differential operational amplifier (±PWM output)

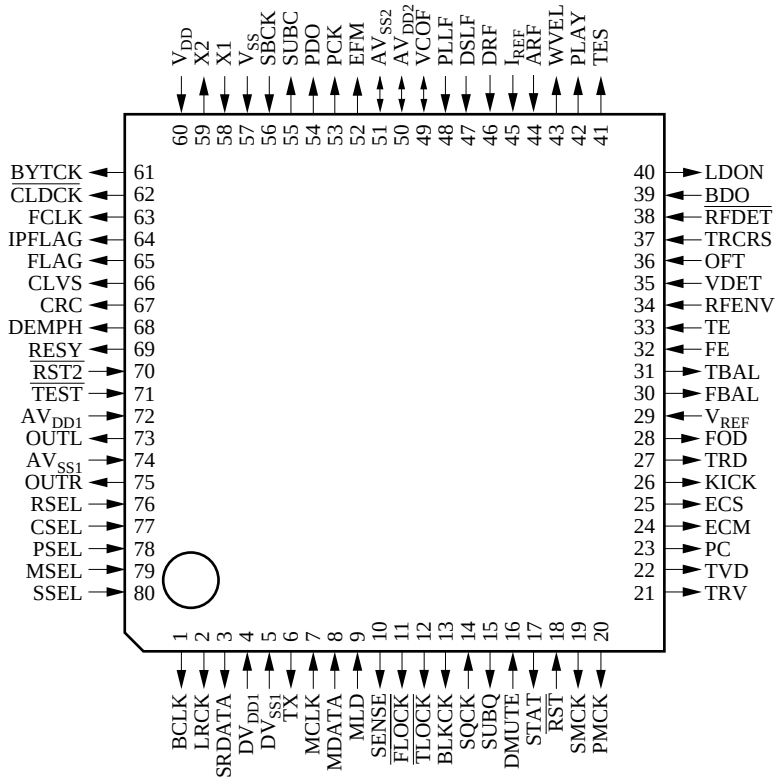
(Other)

- Built-in playback pitch control function (±13%)
- Operating voltage 4.5 to 5.5 V

■ Applications

- CD Players

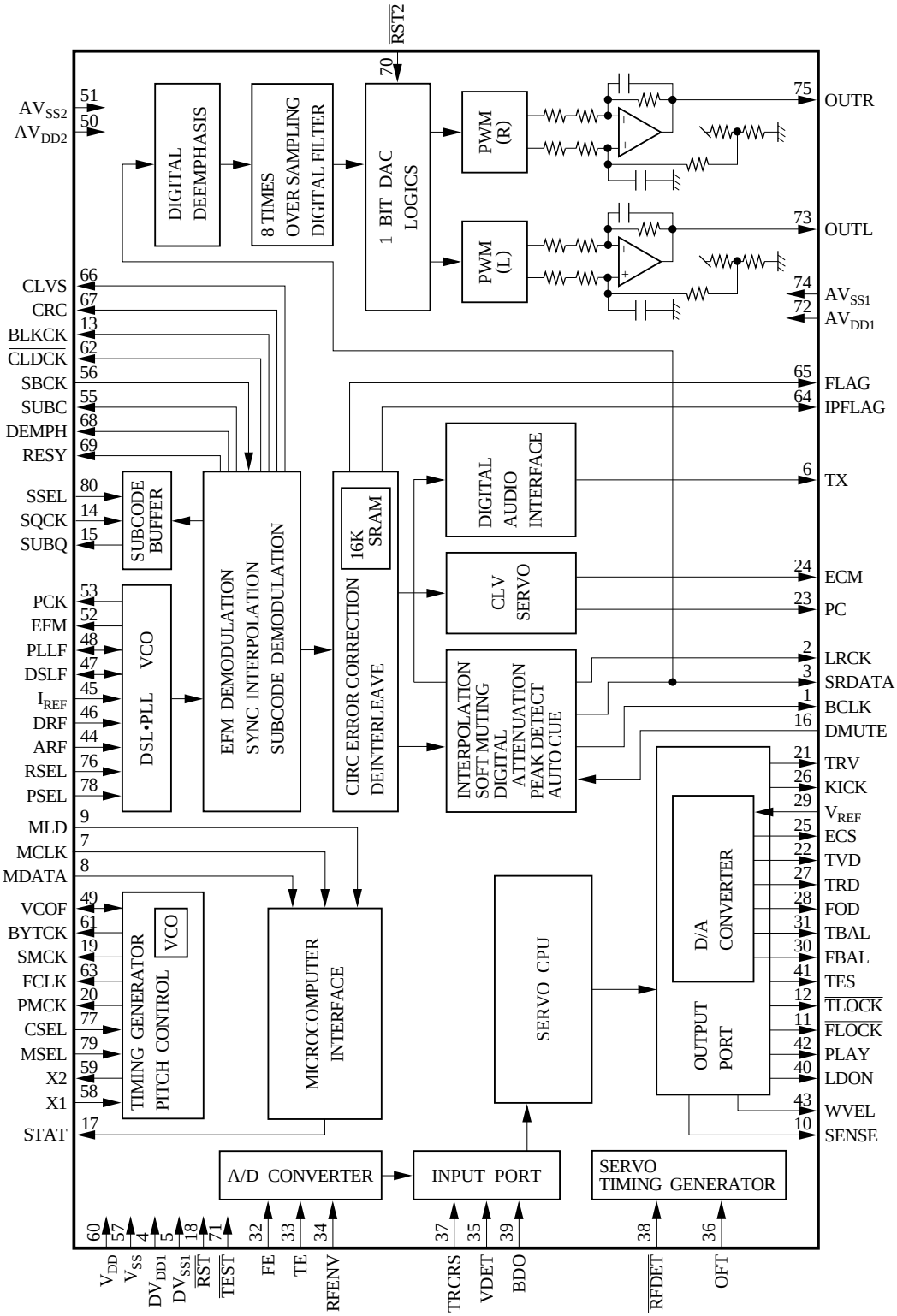
■ Pin Assignment



(TOP VIEW)

QFS080-P-1414

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	I/O	Function Description
1	BCLK	O	SRDATA bit clock output
2	LRCK	O	Left/right channel discrimination signal output
3	SRDATA	O	Serial data output
4	DV_{DD1}	I	Power supply for digital circuits
5	DV_{SS1}	I	Ground for digital circuits
6	TX	O	Digital audio interface output signal
7	MCLK	I	Microcomputer command clock input (Data is latched at rising edge.)
8	MDATA	I	Microcomputer command data input
9	MLD	I	Microcomputer command load signal input. "L" level: load.
10	SENSE	O	Sense signal output (OFT, FESL, NACEND, NAJEND, POSAD, and SFG)
11	$\overline{FLOCK}$	O	Focus servo convergence signal. "L" level: convergence.
12	$\overline{TLOCK}$	O	Tracking servo convergence signal. "L" level: convergence.
13	BLKCK	O	Subcode block clock signal (f_{BLKCK}=75 Hz, normal playback)
14	SQCK	I	External clock input for subcode Q register
15	SUBQ	O	Subcode Q data output
16	DMUTE	I	Muting input. "H" level: muting.
17	STAT	O	Status signal (CRC, CUE, CLVS, TTSTOP, FCLV, and SQOK)
18	$\overline{RST}$	I	Reset input. "L" level: reset.
19	SMCK	O	If MSEL is at "H" level, 8.4672 MHz clock signal output. If MSEL is at "L" level, 4.2336 MHz clock signal output.
20	PMCK	O	88.2 kHz clock signal output
21	TRV	O	Traverse forced feed output
22	TVD	O	Traverse drive output
23	PC	O	Spindle motor ON signal. "L" level: ON.
24	ECM	O	Spindle motor drive signal (forced mode output) 3-State
25	ECS	O	Spindle motor drive signal (servo error signal output)
26	KICK	O	Kick pulse output
27	TRD	O	Tracking drive output
28	FOD	O	Focus drive output
29	V_{REF}	I	Reference voltage for DA output (TVD, ECS, TRD, FOD, FBAL, and TBAL)
30	FBAL	O	Focus balance adjustment output
31	TBAL	O	Tracking balance adjustment output
32	FE	I	Focus error signal input (analog input)
33	TE	I	Tracking error signal input (analog input)
34	RFENV	I	RF envelope signal input (analog input)
35	VDET	I	Vibration detection signal input. "H" level: vibration detected.
36	OFT	I	Offtrack signal input. "H" level: offtrack.
37	TRCRS	I	Track cross signal input
38	$\overline{RFDET}$	I	RF detection signal input. "L" level: detected.
39	BDO	I	Dropout signal input. "H" level: dropout.
40	LDON	O	Laser ON signal output. "H" level: ON.

■ Pin Descriptions (continued)

Pin No.	Symbol	I/O	Function Description
41	TES	O	Tracking error shunt signal. "H" level: shunt.
42	PLAY	O	Play signal output. "H" level: play.
43	WVEL	O	Double-speed status signal output. "L" level: double-speed.
44	ARF	I	RF signal input
45	I_{REF}	I	Reference current input pin
46	DRF	I	DSL bias pin
47	DSLF	I/O	DSL loop filter pin
48	PLLF	I/O	PLL loop filter pin
49	VCOF	I/O	VCO loop filter pin for pitch control
50	AV_{DD2}	I	Power supply for analog circuits (DSL, PLL, and D/A converter output)
51	AV_{SS2}	I	Ground for analog circuits (DSL, PLL, and D/A converter output)
52	EFM	O	EFM signal output
53	PCK	O	PLL derived clock output with f_{PCK}=4.3218 MHz
54	PDO	O	Phase comparator output for EFM and PCK signals
55	SUBC	O	Subcode serial output data output
56	SBCK	I	Serial clock input for subcode serial output
57	V_{SS}	I	Ground for oscillator circuit
58	X1	I	Crystal oscillator circuit input pin. f=16.9344 MHz.
59	X2	O	Crystal oscillator circuit output pin. f=16.9344 MHz.
60	V_{DD}	I	Power supply for oscillator circuit
61	BYTCK	O	Byte clock signal output
62	$\overline{CLDCK}$	O	Subcode frame clock signal output pin (f_{CLDCK}=7.35 kHz)
63	FCLK	O	Crystal frame clock signal output (f_{FCLK}=7.35 kHz)
64	IPFLAG	O	Interpolation flag signal output. "H" level: interpolation.
65	FLAG	O	Flag signal output
66	CLVS	O	Spindle servo phase synchronization signal output. "H" level: CLV. "L" level: rough servo.
67	CRC	O	Subcode CRC check result output. "H" level: OK. "L" level: no good.
68	DEMPH	O	De-emphasis detection signal output. "H" level: ON.
69	RESY	O	Frame resynchronization signal. "H" level: synchronized. "L" level: out of sync.
70	$\overline{RST2}$	I	Reset pin for stopping operation of circuits past D/A converter
71	$\overline{TEST}$	I	Test pin. Keep this pin at "H" level.
72	AV_{DD1}	I	Power supply for analog circuits (common use for by left and right channel audio outputs)
73	OUTL	O	Left channel audio output
74	AV_{SS1}	I	Ground for analog circuits (common use for left and right channel audio outputs)
75	OUTR	O	Right channel audio output
76	RSEL	I	RF signal polarity selection pin. "H" level: bright level is "H. "L" level: bright level is "L.
77	CSEL	I	Test pin. Keep this pin at "L" level.

■ Pin Descriptions (continued)

Pin No.	Symbol	I/O	Function Description
78	PSEL	I	Test pin. Keep this pin at "L" level.
79	MSEL	I	Frequency selection pin for SMCK pin output. "H" level: SMCK=8.4672 MHz. "L" level: SMCK=4.2336 MHz.
80	SSEL	I	SUBQ pin output mode selection pin. "H" level: buffered subcode Q mode.

■ Package Dimensions (Unit: mm)

QFS080-P-1414