

## 8-bit D/A Converter Supporting with I<sup>2</sup>C Bus

### Description

The CXA1315M/P is developed as a 5-channel 8-bit D/A converter supporting with I<sup>2</sup>C bus.

### Features

- Serial control through I<sup>2</sup>C bus
- 5-channel 8-bit D/A converter
- Built-in 4 general-purpose I/O ports (Digital I/O)
- I/O can be specified to respective ports independently
- Selection of 8 slave addresses possible through address select pins (3 pins)

### Applications

The IC, which cannot support I<sup>2</sup>C bus, can support it by connecting its control pin to the CXA1315M/P.

### Structure

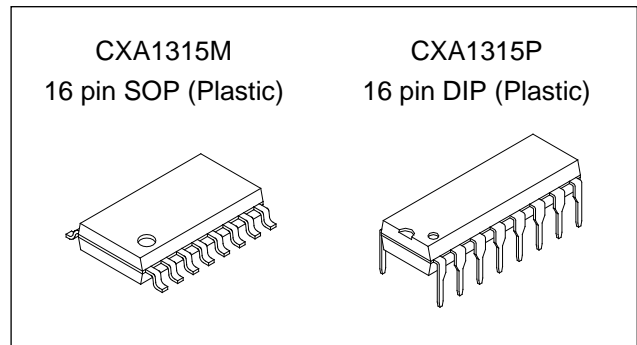
Bipolar silicon monolithic IC

### Absolute Maximum Ratings (Ta = 25°C)

- |                               |                  |             |    |
|-------------------------------|------------------|-------------|----|
| • Supply voltage              | V <sub>CC</sub>  | 12          | V  |
| • Operating temperature       | T <sub>opr</sub> | -20 to +75  | °C |
| • Storage temperature         | T <sub>stg</sub> | -65 to +150 | °C |
| • Allowable power dissipation | P <sub>D</sub>   | 960         | mW |

### Operating Conditions

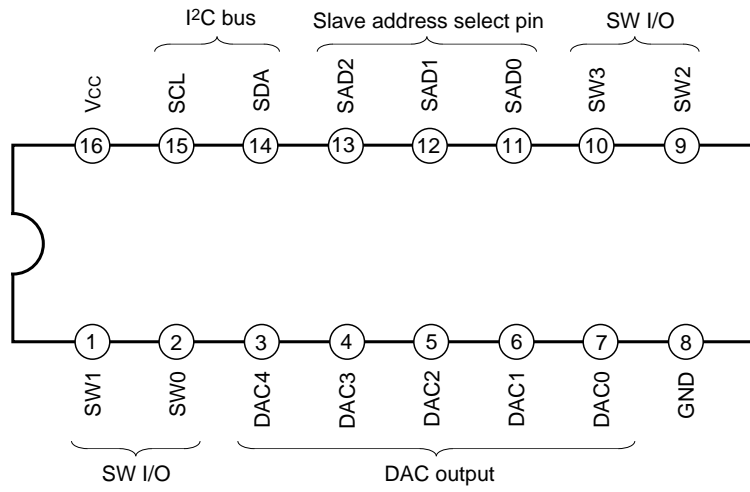
- |                         |                  |            |    |
|-------------------------|------------------|------------|----|
| • Supply voltage        | V <sub>CC</sub>  | 8.2 to 9.8 | V  |
| • Operating temperature | T <sub>opr</sub> | -20 to +75 | °C |



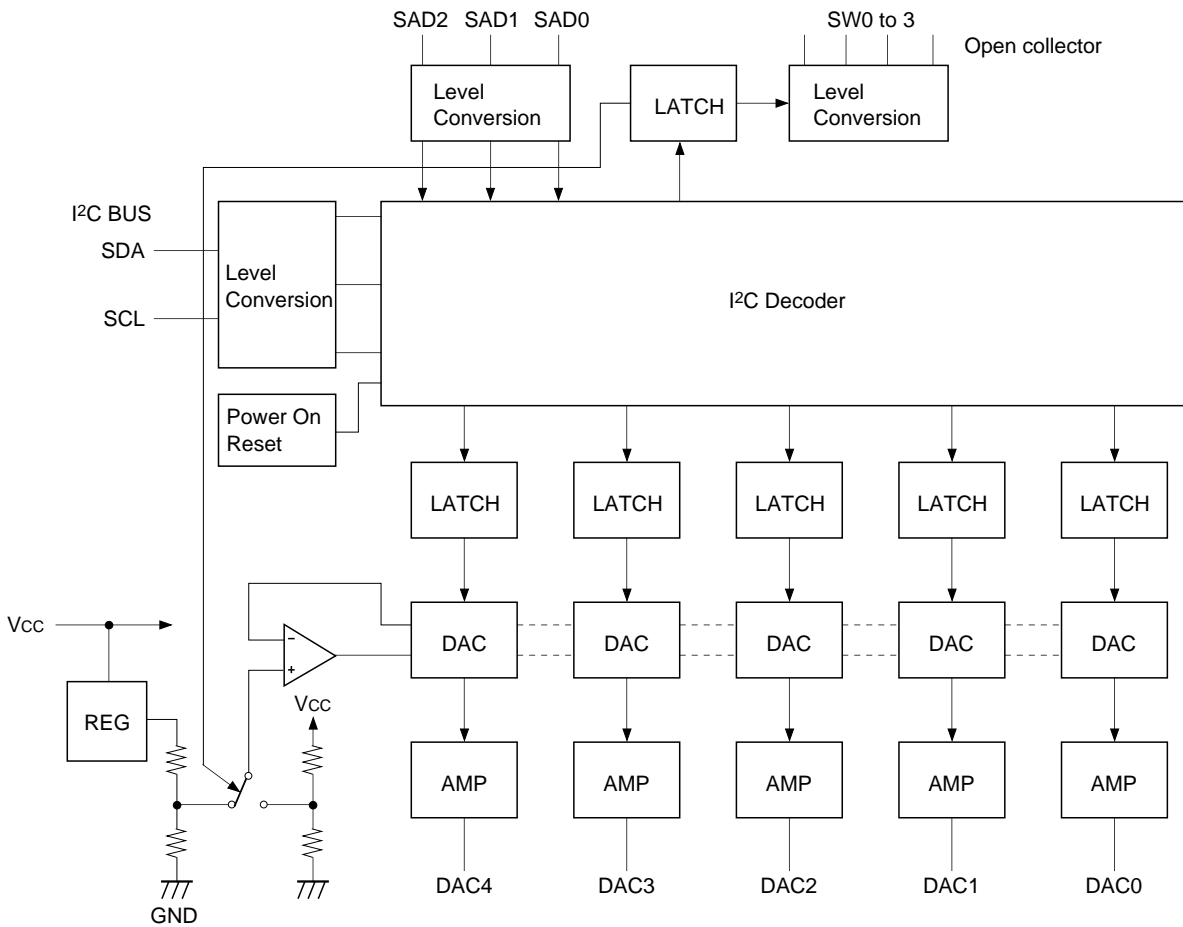
Purchase of Sony's I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specifications as defined by Philips.

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Pin Configuration (Top View)



Block Diagram



Pin Description

No.	Symbol	Equivalent circuit	Description
1 2 9 10	SW1 SW0 SW2 SW3		I/O pin for genera-purpose I/O port $V_{ILmax}: 1.5V$ $V_{IHmin}: 3V$ $V_{OLmax}: 0.4V$
14	SDA		SDA I/O pin for I <sup>2</sup> C bus
3 4 5 6 7	DAC4 DAC3 DAC2 DAC1 DAC0		D/A converter output pin
8	GND		GND pin
11 12 13	SAD0 SAD1 SAD2		Slave address input pin Input at positive logic $V_{ILmax}: 1.5V$ $V_{IHmin}: 3V$
15	SCL		SCL input pin for I <sup>2</sup> C bus
16	Vcc		Power supply pin

Electrical Characteristics

(Ta = 25°C, Vcc = 9V)

No.	Item	Symbol	Test circuit	Test conditions	Min.	Typ.	Max.	Unit
1	Circuit current	Icc	1	DAC 0 to 4 = 127	8	11	15	mA

D/A Converter Block

2	Differential linearity	DLE	1	$\frac{V(\text{DAC0 to 4} = n + 1) - V(\text{DAC0 to 4} = N)}{V(\text{DAC0 to 4} = 191) - V(\text{DAC0 to 4} = 63)} \times 128 - 1$ n = 0 to 127	-1	0	+1.1	LSB
3	Minimum output voltage	Vmin	1	DAC 0 to 4 = 0	0.1	0.4	0.62	V
4	Maximum output voltage	Vmax	1	DAC 0 to 4 = 255	8.3	8.5	8.9	V
5	Output current	Iout	2	Current that can be flowed from Pins 3 to 7	-1		+1	mA
6	Output impedance	Zo	2	DAC 0 to 4 = 127, $\frac{V(-1mA) - V(1mA)}{2mA}$	0	3	6	Ω
7	Reple rejection	Grip	3	DAC 0 to 4 = 127, REF = 0 Superimose 100Hz to Vcc, 1Vp-p	—	-60	-40	dB

**SW, SAD Pins**

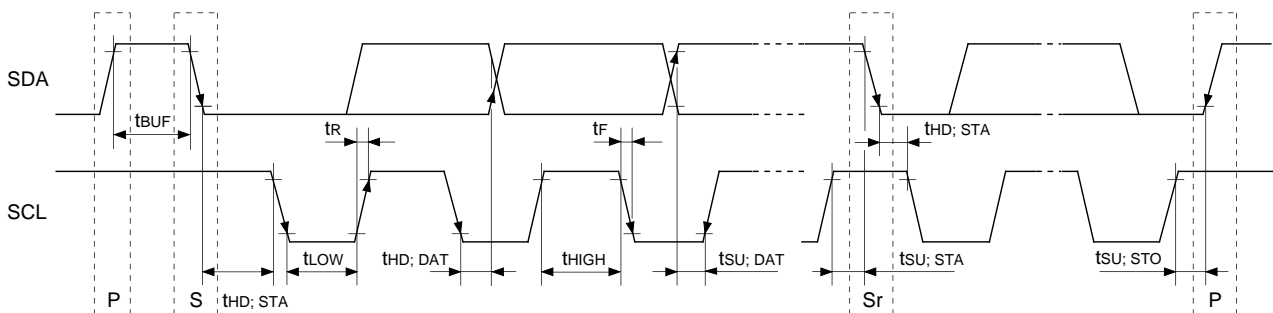
No.	Item	Symbol	Test circuit	Test conditions	Min.	Typ.	Max.	Unit
8	Low level input voltage	$V_{IL}$	4	Input voltage where ST0 to ST3 become "0"	—	—	1.5	V
8	High level input voltage	$V_{IH}$	4	Input voltage where ST0 to ST3 become "1"	3.0	—	—	V
9	Low level input current	$I_{IL}$	4	Input current when 0.4V is applied	-10	0	+10	$\mu$ A
10	High level input current	$I_{IH}$	4	Input current when 4.5V is applied	-10	0	+10	$\mu$ A
11	Low level input voltage	$V_{OL}$	5	SW 0 to 3 = 1, Output voltage when 1mA flows in	0	0.2	0.4	V

**I<sup>2</sup>C Bus Block Items (SDA, SCL)**

No.	Item	Symbol	Min.	Typ.	Max.	Unit
13	High level input voltage	$V_{IH}$	3.0	—	5.0	V
14	Low level input voltage	$V_{IL}$	0	—	1.5	V
15	High level input current	$I_{IH}$	—	—	10	$\mu$ A
16	Low level input current	$I_{IL}$	—	—	10	$\mu$ A
17	Low level output voltage, at 3mA flow to SDA (Pin 14)	$V_{OL}$	0	—	0.4	V
18	Maximum flowing current	$I_{OL}$	3	—	—	mA
19	Input capacitance	$C_i$	—	—	10	pF
20	Maximum clock frequency	$f_{SCL}$	0	—	100	kHz
21	Data change minimum waiting time	$t_{BUF}$	4.7	—	—	$\mu$ s
22	Data transfer start minimum waiting time	$t_{HD; STA}$	4.0	—	—	$\mu$ s
23	Low level clock pulse width	$t_{LOW}$	4.7	—	—	$\mu$ s
24	High level clock pulse width	$t_{HIGH}$	4.0	—	—	$\mu$ s
25	Minimum start preparation waiting time	$t_{SU; STA}$	4.7	—	—	$\mu$ s
26	Minimum data hold time	$t_{HD; DAT}$	5	—	—	$\mu$ s
27	Minimum data preparation time	$t_{SU; DAT}$	250	—	—	ns
28	Rise time	$t_R$	—	—	1	$\mu$ s
29	Fall time	$t_F$	—	—	300	ns
30	Minimum stop preparation waiting time	$t_{SU; STO}$	4.7	—	—	$\mu$ s

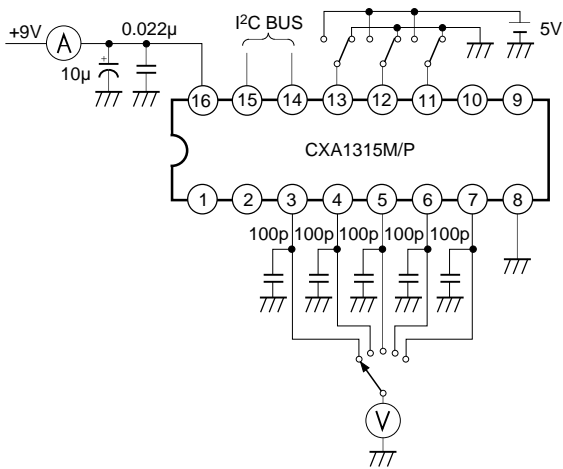
I<sup>2</sup>C bus load conditions: Pull-up resistance 4k $\Omega$  (Connected to +5V)  
 Load capacitance 200pF (Connected to GND)

**I<sup>2</sup>C Bus Control Signal**

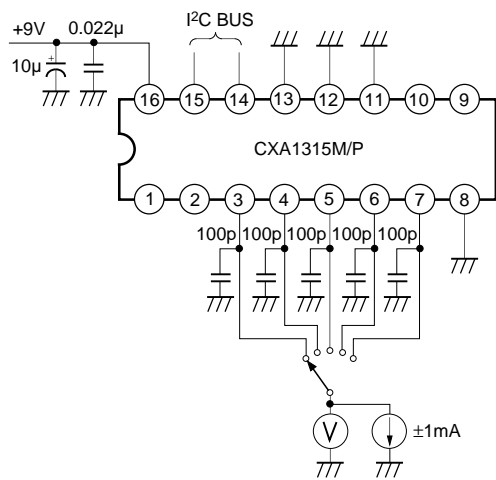


Electrical Characteristics Measurement Circuit

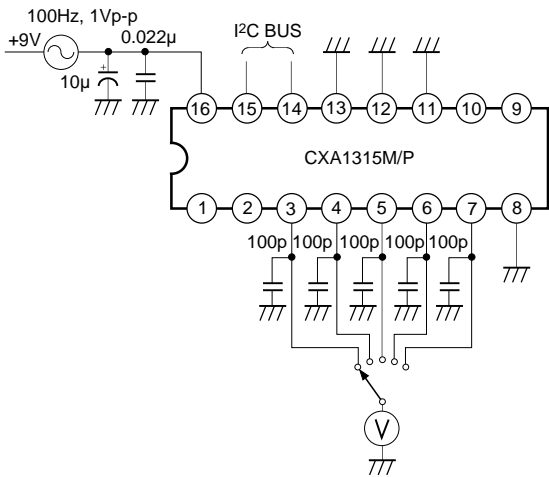
Measurement Circuit 1



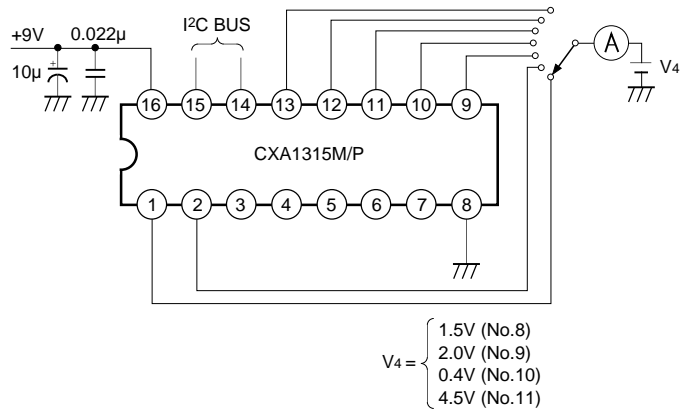
Measurement Circuit 2



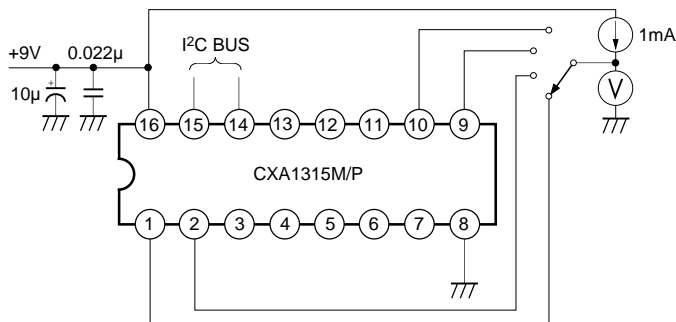
Measurement Circuit 3



Measurement Circuit 4



Measurement Circuit 5





<Registers> In brackets ( ) number of bits

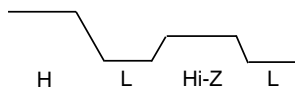
- REF (1): Switches D/A converter reference voltage  
 0: Standardizes the inner regulator  
 1: Standardizes voltage resistance divided from Vcc
- SW0 to 3 (1): Selects ON/OFF of Pins 1, 2, 9 and 10  
 (Each pin is the open collector output of NPN transistor)  
 0: OFF  
 1: ON
- DAC0 to 4 (8): Digital data input register of D/A converter  
 0: Output voltage turns to minimum  
 255: Output voltage turns to maximum
- PONRES (1): Detects POWER ON RESET  
 0: Master passes from the bus and is reset to "0" after having read this status  
 1: Sets to "1" when power supply is turned on or when there has been a power dip
- ST0 to 3 (1): Detects and registers the voltage condition of Pins 1, 2, 9 and 10  
 0: 1.5V and below  
 1: 3.0V and above  
**Note)** SW0 to 3 effective during "0"

## I<sup>2</sup>C Bus Signal

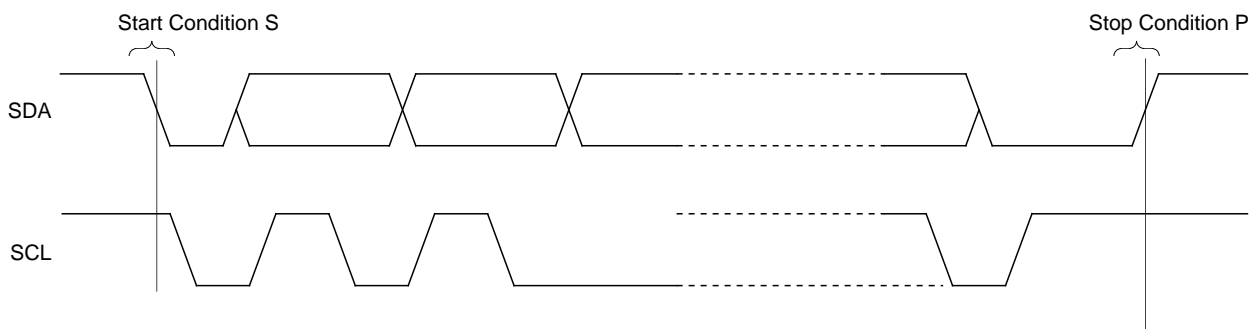
There are 2 signals in I<sup>2</sup>C bus. SDA (Serial Data) and SCL (Serial Clock).

SDA is double-way.

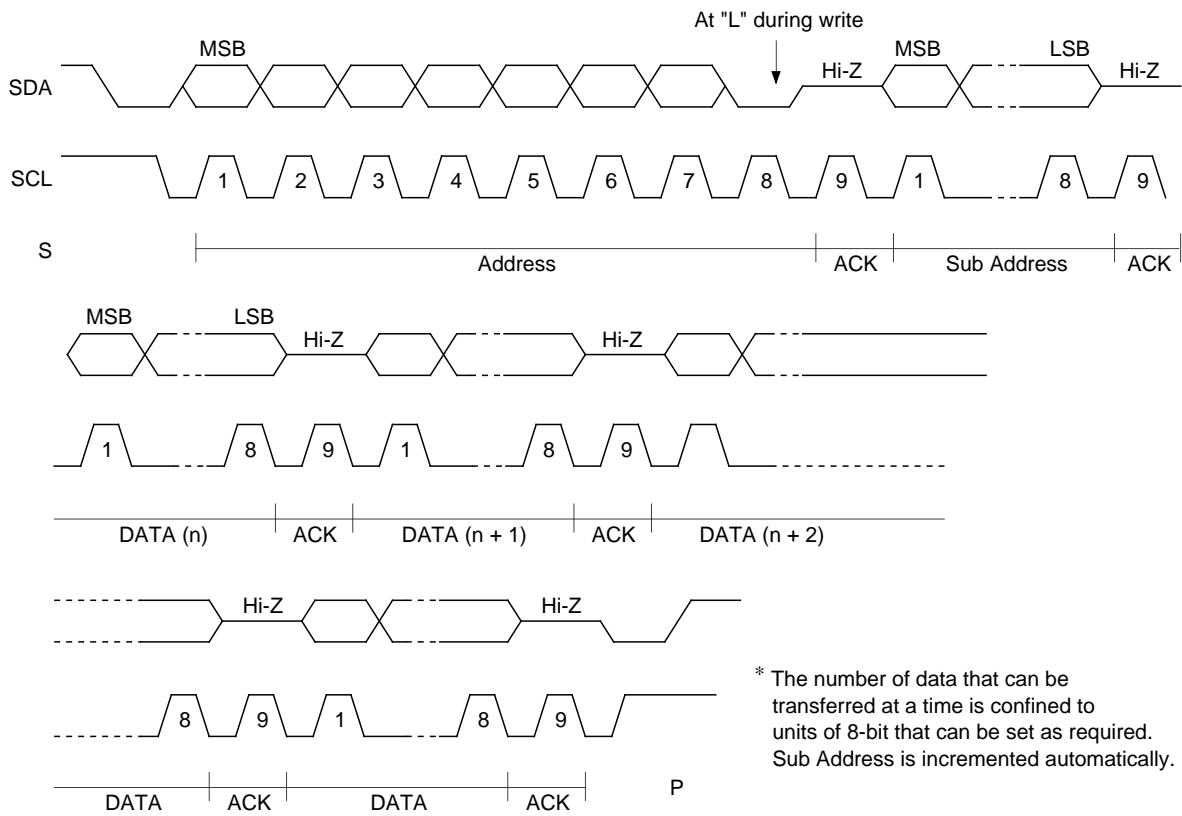
- As SDA is bidirectional it has 3 state outputs, H, L and Hi-Z.



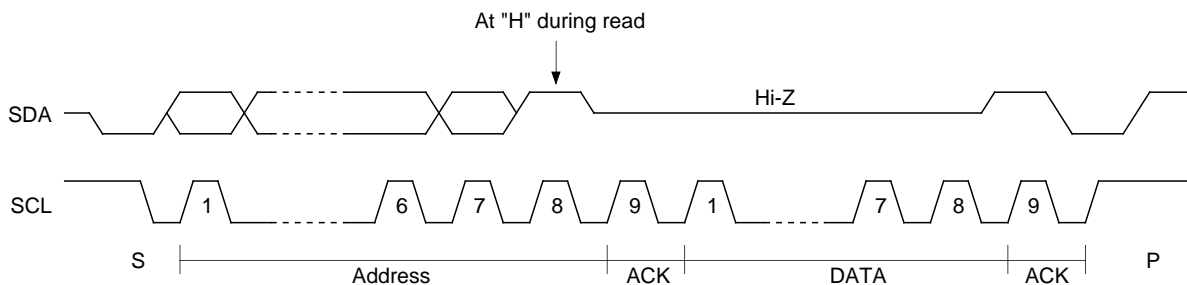
- I<sup>2</sup>C transfer begins with Start Condition S and ends with Stop Condition P.



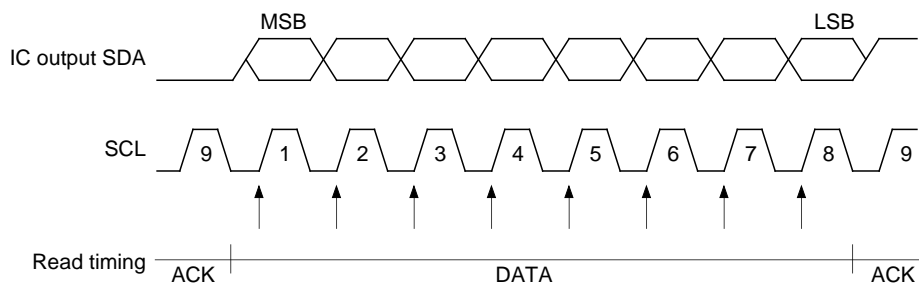
• I<sup>2</sup>C data write (Write from I<sup>2</sup>C controller to IC)



• I<sup>2</sup>C data read (Read from IC to I<sup>2</sup>C controller)



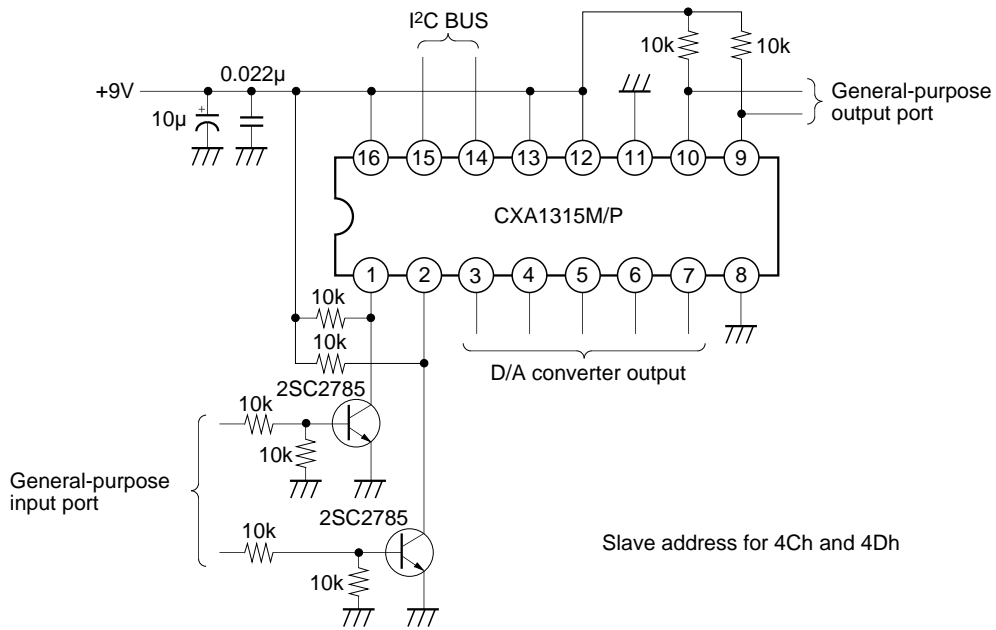
• Read timing



\* Data read is performed with SCL rise.

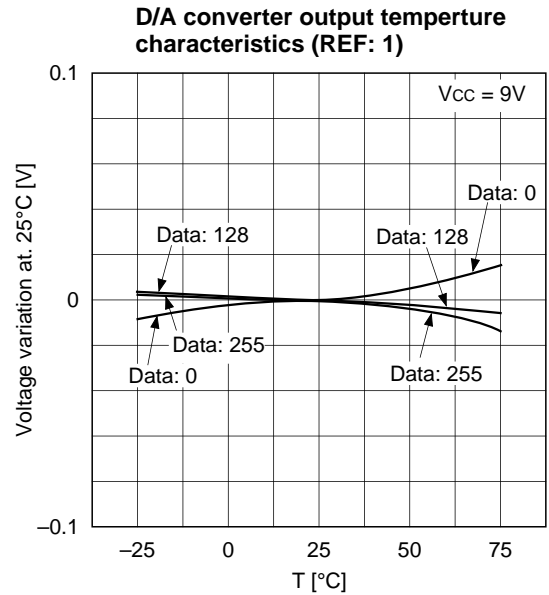
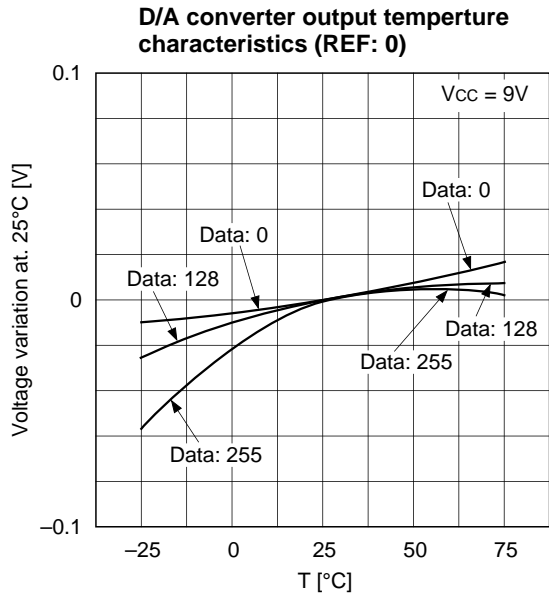


Application Circuit



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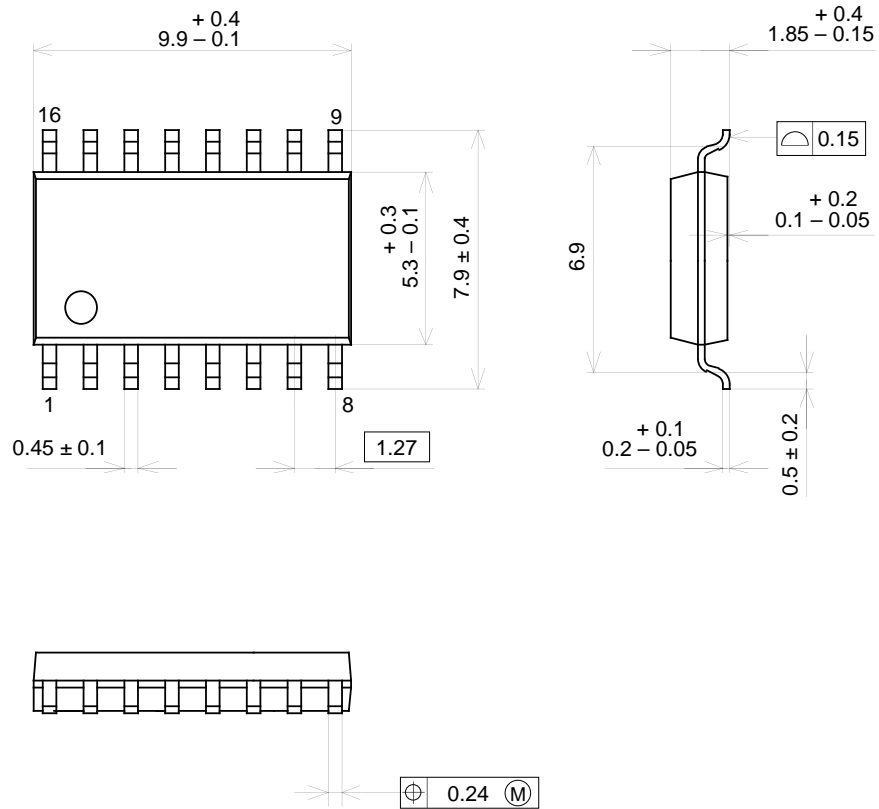
Characteristics Diagram



Package Outline Unit: mm

CXA1315M

16PIN SOP (PLASTIC)



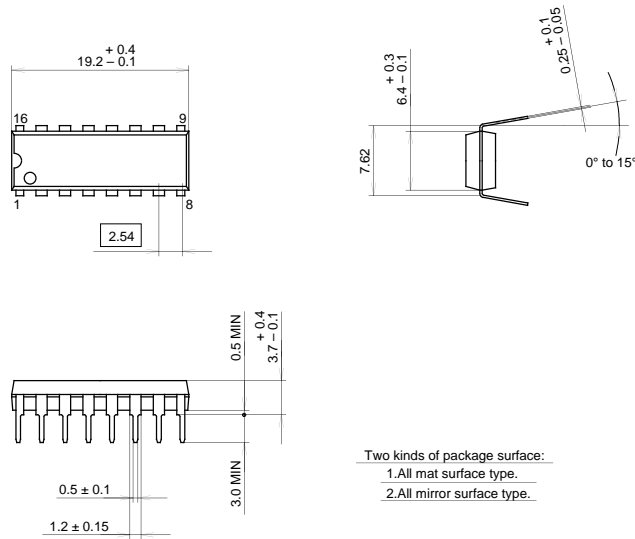
PACKAGE STRUCTURE

SONY CODE	SOP-16P-L01
EIAJ CODE	SOP016-P-0300
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.2g

CXA1315P

16PIN DIP (PLASTIC)

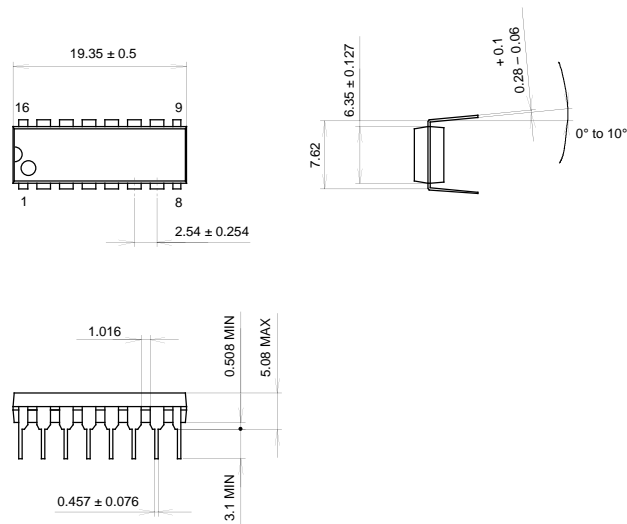


PACKAGE STRUCTURE

SONY CODE	DIP-16P-01
EIAJ CODE	DIP016-P-0300
JEDEC CODE	Similar to MO-001-AE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	1.0 g

16PIN DIP (PLASTIC) 300mil



PACKAGE STRUCTURE

SONY CODE	DIP-16P-191
EIAJ CODE	DIP016-P-0300-AU
JEDEC CODE	MS-001-AA

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER
PACKAGE WEIGHT	1.0g