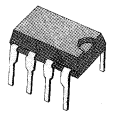
JFET-INPUT DUAL OPERATIONAL AMPLIFIERS

- HIGH SLEW-RATE ... 13V/μs TYP.
- LOW POWER CONSUMPTION
- WIDE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW INPUT BIAS AND OFFSET CURRENTS
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE ... JFET-INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH-UP-FREE OPERATION

The MC34002 JFET-input operational amplifiers are designed to offer high slew-rate, low input bias and offset current, and low offset voltage temperature coefficient. Each JFET-input operational amplifier incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.

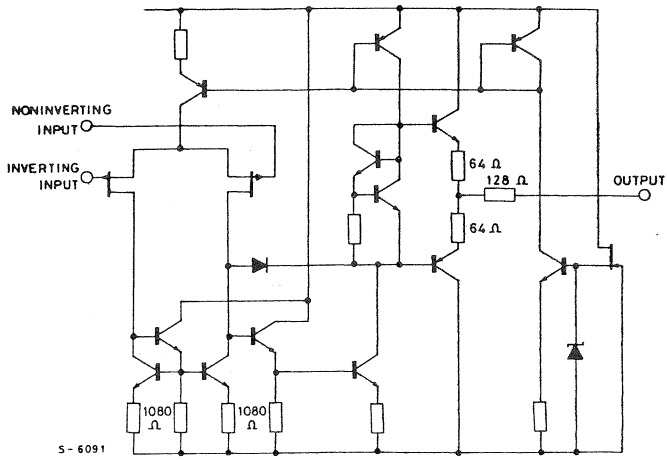


Minidip
(Plastic and Ceramic)

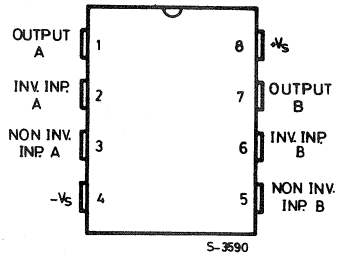
ABSOLUTE MAXIMUM RATINGS

V_s	Supply voltage	+ 18	V
V_{is}	Differential input voltage	± 30	V
V_i	Input voltage	± 16	V
T_{op}	Operating ambient temperature	0 to 70	°C
T_j	Operating junction temperature	115	°C
T_{stg}	Storage temperature	-65 to 150	°C

SCHEMATIC DIAGRAM
(one section)



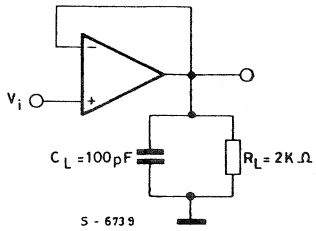
CONNECTION DIAGRAM
(Top view)



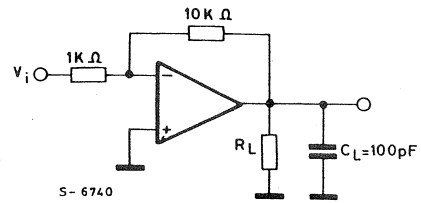
ORDERING NUMBERS

TYPE	PACKAGE	
	Plastic Minidip	Ceramic Minidip
MC34002	MC34002P	MC34002U
MC34002A	MC34002 AP	MC34002 AU
MC34002B	MC34002 BP	MC34002 BU

TEST CIRCUITS



Unity gain amplifier



Gain of 10 inverting amplifier

THERMAL DATA

			Plastic Minidip	Ceramic Minidip
$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max	120°C/W	150°C/W

ELECTRICAL CHARACTERISTICS ($V_s = \pm 15V$, $T_{amb} = 25°C$, otherwise specified)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit
V_{OS}	Input offset voltage	$R_s < 10K\Omega$	MC34002A		1	2	mV
			MC34002B		3	5	
			MC34002		5	10	
		$R_s < 10K\Omega$, T_{amb} = full range	MC34002A			4	
			MC34002B			7	
			MC34002			13	
$\frac{\Delta V_{OS}}{\Delta T}$	Input offset voltage drift	$R_s < 10K\Omega$, T_{amb} = full range			10		$\mu V/°C$
I_{OS}	Input offset current		MC34002A		25	50	pA
			MC34002B		25	100	
			MC34002		25	100	
		T_{amb} = full range	MC34002A			2	nA
			MC34002B			4	
			MC34002			4	
I_b	Input bias current		MC34002A		50	100	pA
			MC34002B		50	200	
			MC34002		50	200	
		T_{amb} = full range	MC34002A			4	nA
			MC34002B			8	
			MC34002			8	
V_{CM}	Common mode input voltage range			+ 11	+ 15 + 12		V
		T_{amb} = full range		± 11			
V_{OPP}	Large signal voltage swing		$R_L > 10K\Omega$	± 12	± 14		V
			$R_L > 2K\Omega$	± 10	± 13		
		T_{amb} = full range	$R_L > 10K\Omega$	± 12			
			$R_L > 2K\Omega$	± 10			
G_V	Large signal voltage gain	$R_L \geq 2K\Omega$, $V_o = \pm 10V$	MC34002A	50	150		V/mV
			MC34002B	50	150		
			MC34002	25	100		
		$R_L \geq 2K\Omega$, $V_o = \pm 10V$	MC34002A	25			
			MC34002B	25			
		T_{amb} = full range	MC34002	25			
B	Unity gain bandwidth				4		MHz
R_i	Input resistance				10^{12}		Ω
CMR	Common mode rejection	$R_s < 10K\Omega$	MC34002A	80	100		dB
			MC34002B	80	100		
			MC34002	70	100		
		T_{amb} = full range	MC34002A	80			
			MC34002B	80			
			MC34002	70			

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test Conditions		Min.	Typ.	Max.	Unit.
SVR	Suplly voltage rejection	$R_s < 10K\Omega$	MC34002A	80	100		dB
			MC34002B	80	100		
			MC34002	70	100		
		T_{amb} = full range	MC34002A	80			
			MC34002B	80			
			MC34002	70			
I_S	Supply current	$R_L = \infty$	MC34002A		2.8	5	mA
			MC34002B		2.8	5	
			MC34002		2.8	5.4	
		$R_L = \infty$ T_{amb} = full range	MC34002A			5.6	
			MC34002B			5.6	
			MC34002			6.0	
SR	Slew-rate at unity gain	V_I = 10V C_L = 100pF	R_L = 2KΩ		13		V/μs
e_N	Total input noise voltage	f = 1KHz			25		$\frac{nV}{\sqrt{Hz}}$
i_N	Total input noise current				0.01		$\frac{pA}{\sqrt{Hz}}$

Fig. 1 - Maximum peak to peak output voltage vs. frequency

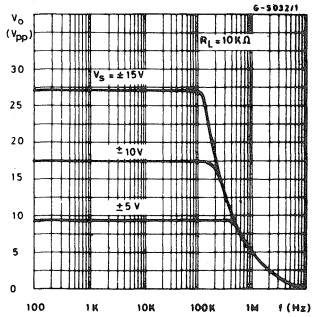


Fig. 2 - Maximum peak to peak output voltage vs. frequency

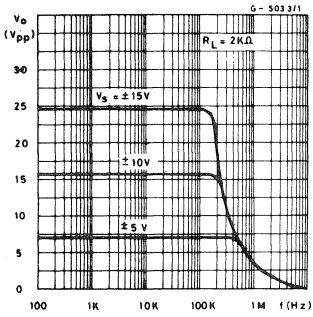


Fig. 3 - Maximum peak to peak output voltage vs. load resistance

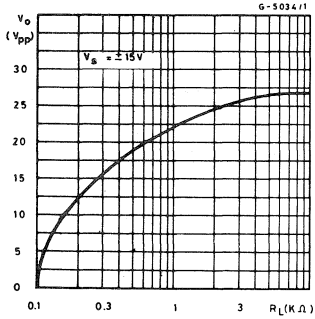


Fig. 4 - Large signal voltage gain and phase shift vs. frequency

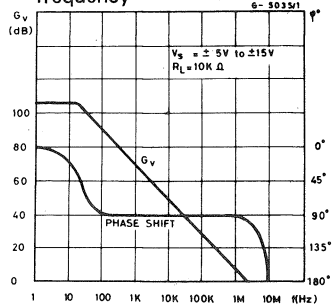


Fig. 5 - Supply current vs. temperature

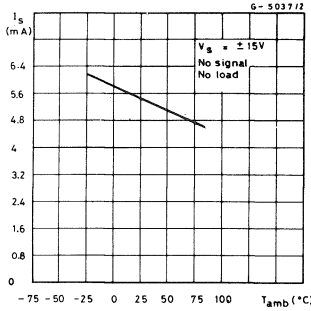


Fig. 6 - Supply current vs. supply voltage

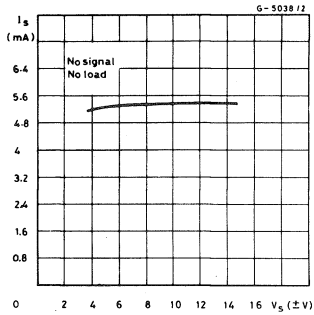


Fig. 7 - Input bias current vs. temperature

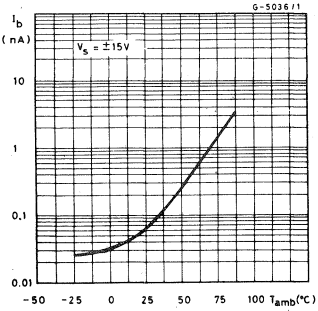


Fig. 8 - Equivalent input noise voltage vs. frequency

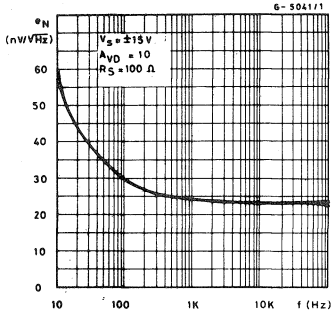
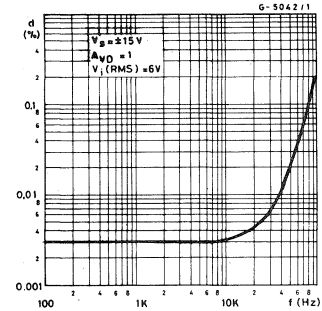
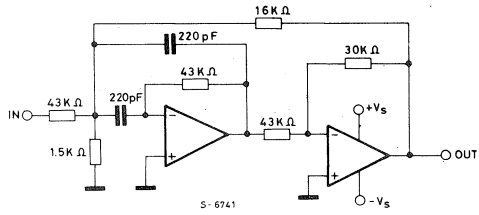


Fig. 9 - Total harmonic distortion vs. frequency



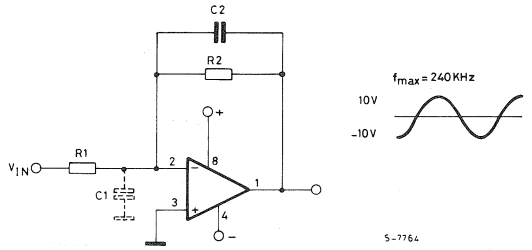
APPLICATION INFORMATION

Fig. 10 - Second order high Q band pass filter (f_o = 100KHz, Q = 30, gain = 4)



APPLICATION INFORMATION (continued)

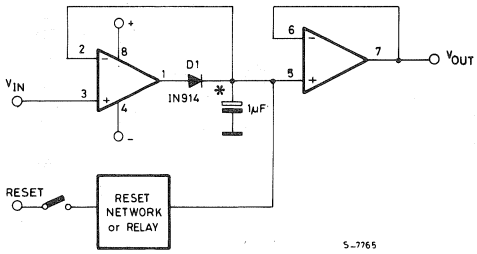
Fig. 11 Wide BW, low noise, low drift amplifier



- Power BW: $f_{max} = \frac{S_r}{2 \pi Vp} \cong 240kHz$

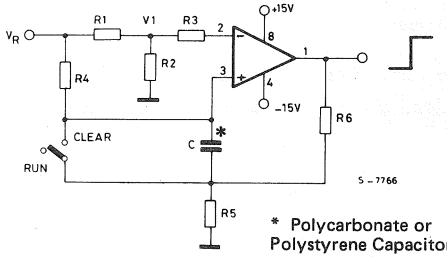
- Parasitic input capacitance (C1 ≅ 3pF plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To comparate add C2 such that: R2C2 ≅ R1C1

Fig. 12 - Positive peak detector



* Polycarbonate capacitor
D1 = Hi-speed, low-reverse leakage diode

Fig. 13 - Long interval RC timer



* Polycarbonate or Polystyrene Capacitor

Time (t) = R4 C ℓn (V_R/V_R-V_I), R3 - R4, R5 - 0.1 R6 if R1 = R2; t = 0.693 R4C

Design Example: 100 Second Timer

V_R = 10V	C = 1.0µF	R3 = R4 = 144M
R6 = 20k	R5 = 2.0k	R1 = R2 = 1.0k

Fig. 14 - 20Hz to 200Hz variable High-pass filter (G_v = 3dB)

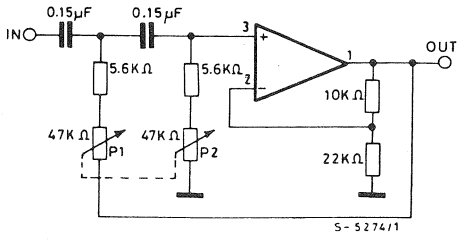


Fig. 15 - Frequency response of the high-pass filter of fig. 17

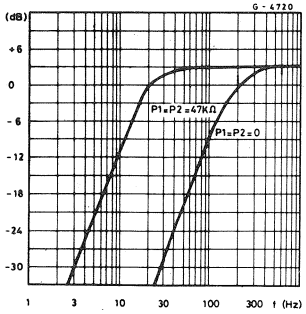
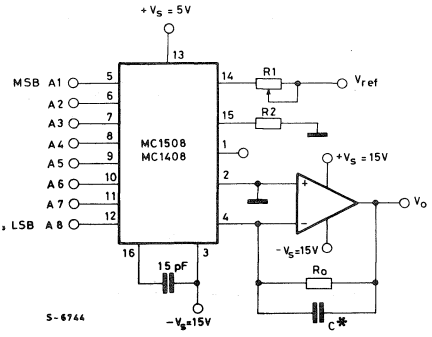


Fig. 16 - Output current to voltage transformation for a DA converter



(*) The value of C may be selected to minimize overshoot and ringing (C ≈ 68 pF).

Settling time to within 1/2 LSB (± 19.5 mV) is approximately 4.0 μs from the time all bits are switched.

Theoretical V_o :

$$V_o = \frac{V_{ref}}{R1}(R_o)\left[\frac{A1}{2}+\frac{A2}{4}+\frac{A3}{8}+\frac{A4}{16}+\frac{A5}{32}+\frac{A6}{64}+\frac{A7}{128}+\frac{A8}{256}\right]$$

Adjust V_{ref}, R1 or R_o so that V_o with all digital inputs at high level is equal to 9.961 volts.

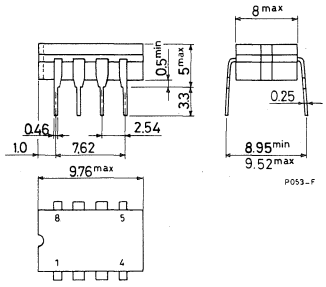
$V_{ref} = 2.0\ V_{dc}$
$R1 = R2 \approx 1.0\ k\Omega$
$R_o = 5.0\ k\Omega$

$$V_o = \frac{2\ V}{1\ k}(5\ k)\left[\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\dots\right]$$

$$= 10V\left[\frac{255}{256}\right] = 9.961V$$

MECHANICAL DATA (Dimensions in mm)

Minidip (Ceramic)



Minidip (Plastic)