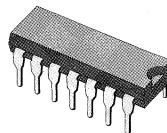


# LINEAR INTEGRATED CIRCUITS

## JFET-INPUT QUAD OPERATIONAL AMPLIFIERS

- HIGH SLEW-RATE ...  $13V/\mu s$  TYP.
- LOW POWER CONSUMPTION
- WIDE COMMON-RANGE AND DIFFERENTIAL VOLTAGE RANGES
- LOW INPUT BIAS AND OFFSET CURRENTS
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE ... JFET-INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH-UP-FREE OPERATION

The MC34004 JFET-input operational amplifiers are designed to offer high slew-rate, low input bias and offset current, and low offset voltage temperature coefficient. Each JFET-input operational amplifier incorporates well-matched, high-voltage JFET and bipolar transistors in a monolithic integrated circuit.



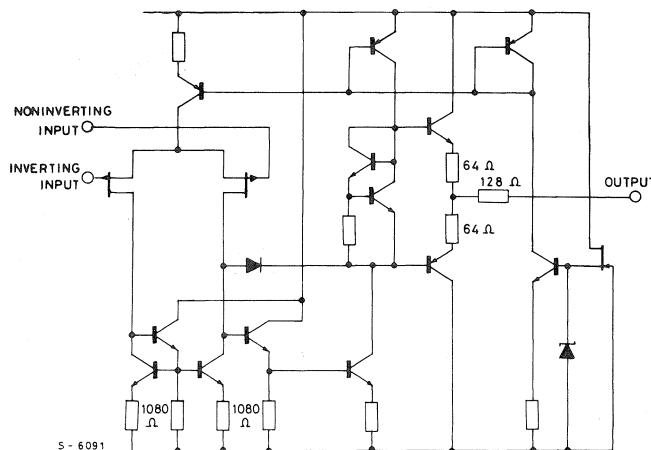
**DIP-14  
(Plastic and Ceramic)**

## ABSOLUTE MAXIMUM RATINGS

$V_s$	Supply voltage	$\pm 18$	V
$V_{is}$	Differential input voltage	$\pm 30$	V
$V_i$	Input voltage	$\pm 16$	V
$T_{op}$	Operating ambient temperature	0 to 70	$^{\circ}\text{C}$
$T_j$	Operating junction temperature	115	$^{\circ}\text{C}$
$T_{stg}$	Storage temperature	-65 to 150	$^{\circ}\text{C}$

## SCHEMATIC DIAGRAM

(one section)

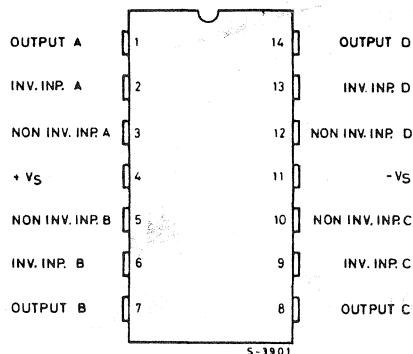




**MC34004**

## CONNECTION DIAGRAM

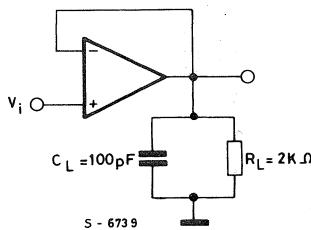
(top view)



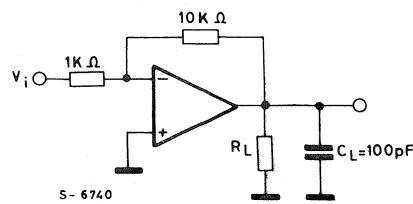
## ORDERING NUMBERS

TYPE	PACKAGE	
	Plastic DIP-14	Ceramic DIP-14
MC34004	MC34004P	MC34004L
MC34004A	MC34004 AP	MC34004 AL
MC34004B	MC34004 BP	MC34004 BL

## TEST CIRCUITS



Unity gain amplifier



Gain of 10 inverting amplifier

## THERMAL DATA

R <sub>th</sub> j-amb	Thermal resistance junction-ambient	max	Ceramic DIP-14	Plastic DIP-14
			150°C/W	200°C/W



MC34004

ELECTRICAL CHARACTERISTICS ( $V_s = \pm 15V$ ,  $T_{amb} = 25^\circ C$ , otherwise specified)

Parameter	Test Conditions		Min.	Typ.	Max.	Unit
$V_{OS}$ Input offset voltage	$R_s < 10K\Omega$	MC34004A		1	2	mV
		MC34004B		3	5	
		MC34004		5	10	
	$R_s < 10K\Omega$ $T_{amb} = \text{full range}$	MC34004A		4		
		MC34004B		7		
		MC34004		13		
$\frac{\Delta V_{OS}}{\Delta T}$ Input offset voltage drift	$R_s < 10K\Omega$ $T_{amb} = \text{full range}$			10		$\mu V/^{\circ}C$
$I_{OS}$ Input offset current		MC34004A		25	50	pA
		MC34004B		25	100	
		MC34004		25	100	
	$T_{amb} = \text{full range}$	MC34004A		2		nA
		MC34004B		4		
		MC34004		4		
$I_b$ Input bias current		MC34004A		50	100	pA
		MC34004B		50	200	
		MC34004		50	200	
	$T_{amb} = \text{full range}$	MC34004A		4		nA
		MC34004B		8		
		MC34004		8		
$V_{CM}$ Common mode input voltage range			11	15		V
	$T_{amb} = \text{full range}$		$\pm 11$	12		
$V_{OPP}$ Large signal voltage swing	$R_L > 10K\Omega$		$\pm 12$	$\pm 14$		V
			$\pm 10$	$\pm 13$		
	$T_{amb} = \text{full range}$	$R_L > 10K\Omega$	$\pm 12$			
		$R_L > 2K\Omega$	$\pm 10$			
$G_V$ Large signal voltage gain	$R_L \geq 2K\Omega$ $V_o = \pm 10V$	MC34004A	50	150		V/mV
		MC34004B	50	150		
		MC34004	25	100		
	$R_L \geq 2K\Omega$ $V_o = \pm 10V$ $T_{amb} = \text{full range}$	MC34004A	25			
		MC34004B	25			
		MC34004	25			
B Unity gain bandwidth				4		MHz
$R_I$ Input resistance				$10^{12}$		$\Omega$
CMR Common mode rejection	$R_s < 10K\Omega$	MC34004A	80	100		dB
		MC34004B	80	100		
		MC34004	70	100		
	$T_{amb} = \text{full range}$	MC34004A	80			
		MC34004B	80			
		MC34004	70			

## ELECTRICAL CHARACTERISTICS (continued)

Parameter	Test Conditions		Min.	Typ.	Max.	Unit
SVR Supply voltage rejection	$R_s < 10\text{ k}\Omega$	MC34004A	80	100		dB
		MC34004B	80	100		
		MC34004	70	100		
	$T_{amb} = \text{full range}$	MC34004A	80			
		MC34004B	80			
		MC34004	70			
$I_s$ Supply current	$R_L = \infty$	MC34004A		5.6	10	mA
		MC34004B		5.6	10	
		MC34004		5.6	10.8	
	$R_L = \infty$ $T_{amb} = \text{full range}$	MC34004A			11.2	
		MC34004B			11.2	
		MC34004			12	
SR Slew-rate at unity gain	$V_i = 10\text{ V}$ $C_L = 100\text{ pF}$	$R_L = 2\text{ k}\Omega$		13		$\text{V}/\mu\text{s}$
$\theta_N$ Total input noise voltage	$f = 1\text{ KHz}$			25		$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
$i_N$ Total input noise current					0.01	$\frac{\text{pA}}{\sqrt{\text{Hz}}}$

Fig. 1 - Maximum peak to peak output voltage vs. frequency

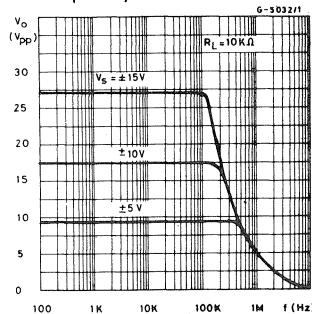


Fig. 2 - Maximum peak to peak output voltage vs. frequency

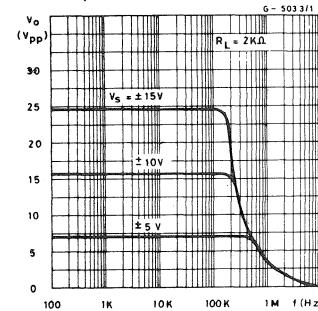
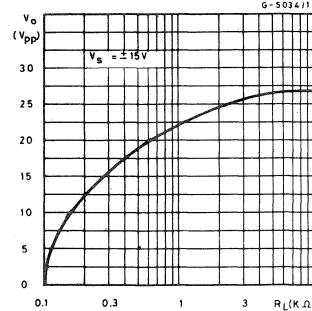
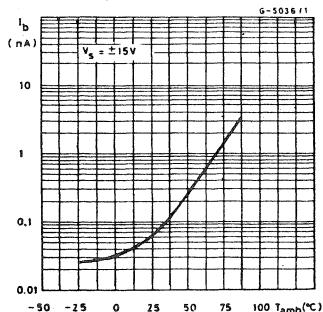


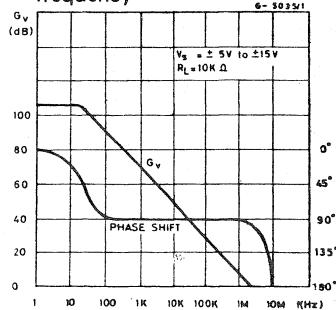
Fig. 3 - Maximum peak to peak output voltage vs. load resistance



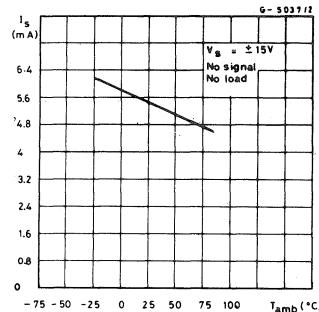
**Fig. 4 - Input bias current vs. temperature**



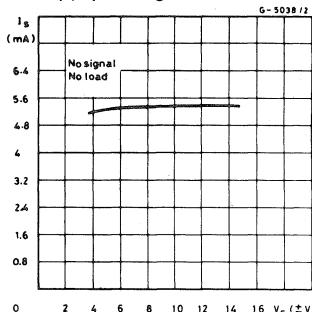
**Fig. 7 - Large signal voltage gain and phase shift vs. frequency**



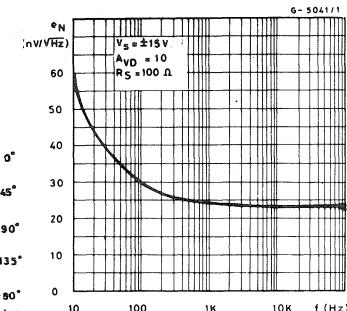
**Fig. 5 - Supply current vs. temperature**



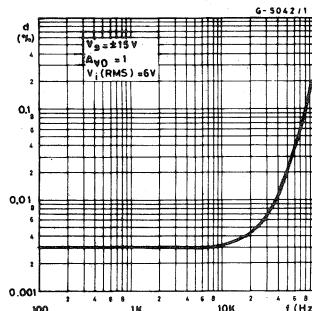
**Fig. 6 - Supply current vs. supply voltage**



**Fig. 8 - Equivalent input noise voltage vs. frequency**

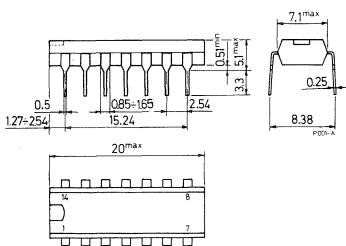


**Fig. 9 - Total harmonic distortion vs. frequency**



## MECHANICAL DATA (Dimensions in mm)

**DIP-14 (Plastic)**



**DIP-14 (Ceramic)**

