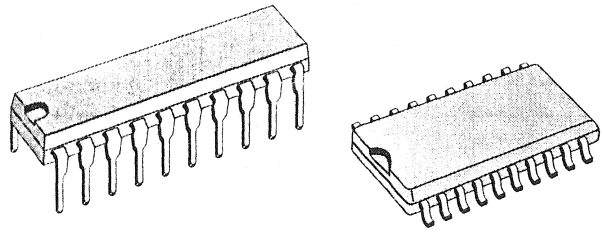
SGS-THOMSON MICROELECTRONICS

TDA7330

SINGLE CHIP RDS DEMODULATOR + FILTER

ADVANCE DATA

- HIGH PERFORMANCE, STABLE 57KHz FILTER
- FILTER ADJUSTMENT FREE AND WITHOUT EXTERNAL COMPONENTS
- PURELY DIGITAL RDS DEMODULATION WITHOUT EXTERNAL COMPONENTS
- ARI OUTPUT (SK INDICATION)
- RDS SIGNAL QUALITY OUTPUT
- 4.332MHz CRYSTAL OSCILLATOR (8.664MHz OPTIONAL)
- LOW NOISE MIXED BIPOLAR/CMOS TECHNOLOGY



DIP20 **SO20**

ORDERING NUMBERS:

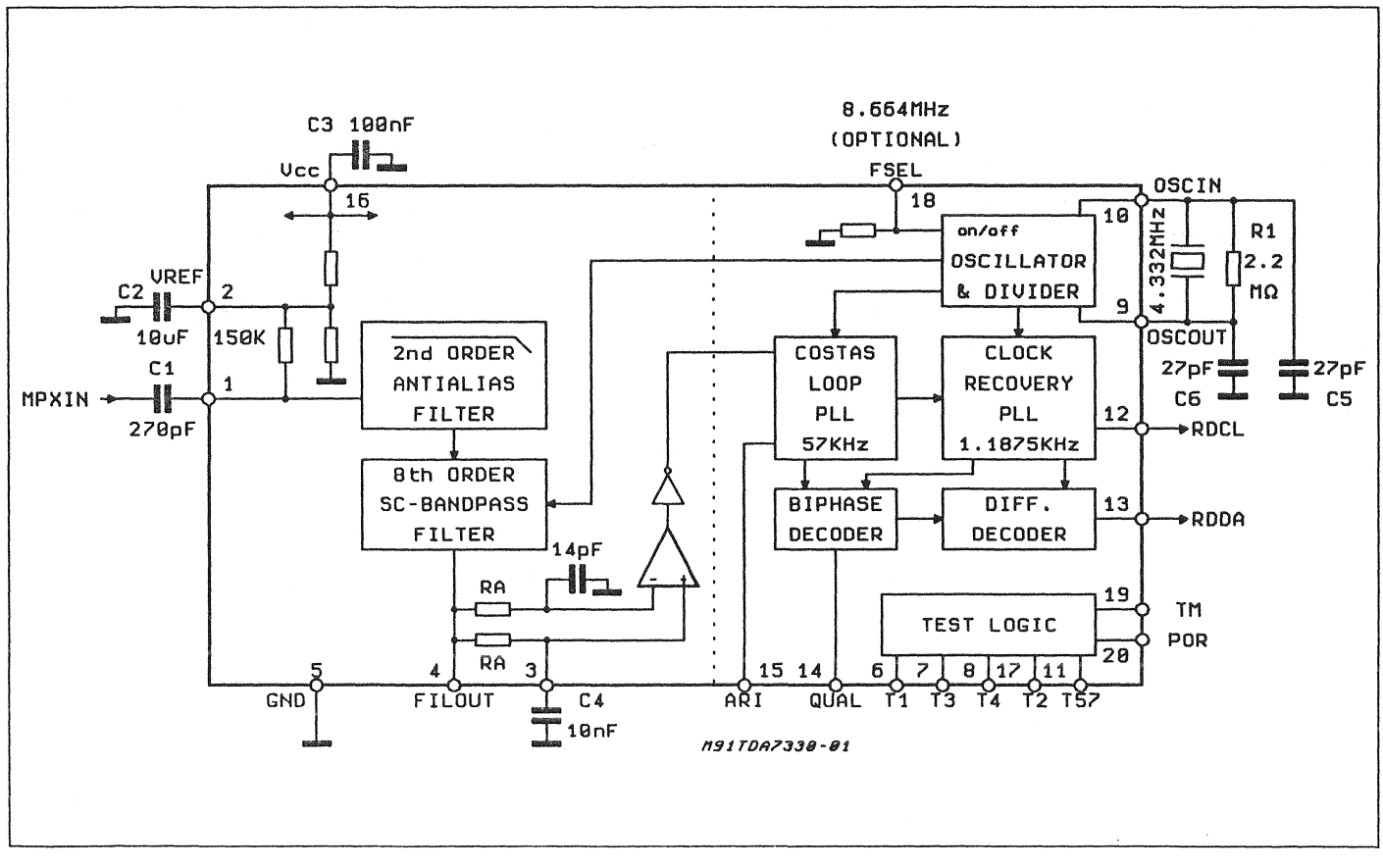
TDA7330 TDA7330D

DESCRIPTION

The TDA7330 is a RDS (Radio Data System) demodulator. The IC includes a 57KHz switched capacitor input band pass filter, a bit rate clock recovery circuit, DSB demodulator circuit, BI-PHASE PSK decoder, differential decoding circuit, ARI identification and signal quality outputs.

The data and clock output signal (RDDA, RDCL) can be further processed by a suitable µP.

BLOCK DIAGRAM



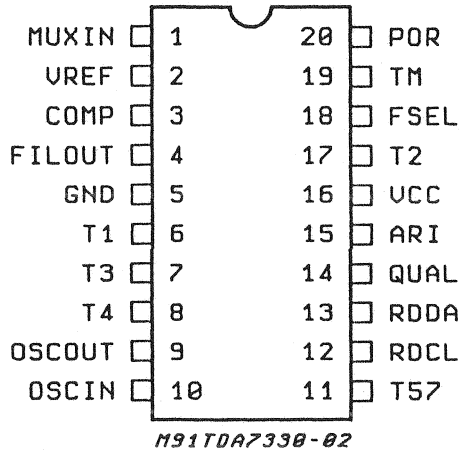
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	7	V
T_{op}	Operating Temperature Range	-40 to 85	°C
T_{stg}	Storage Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Description		DIP20	SO20	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Typ.	100	200	°C/W

PIN CONNECTION (Top view)



PIN FUNCTION

Nr.	Name	Description
1	MUXIN	RDS input signal.
2	V_{ref}	Reference voltage
3	COMP	Not inverting comparator input (smoothing filter)
4	FIL OUT	Filter Output
5	GND	Ground
6	T1	Testing output pin (not to be used)
7	T3	Testing output pin (not to be used)
8	T4	Testing output pin (not to be used)
9	OSC OUT	Oscillator output
10	OSC IN	Oscillator Input
11	T57	Testing output pin (not to be used)
12	RDCL	RDS clock output
13	RDDA	RDS data output
14	QUAL	Output for signal quality indication (High = good)
15	ARI	Output for ARI indication (High when RDS + ARI signal is present) (High when only ARI is present) (Low when only RDS is present) (indefined when no signal is present)
16	V_{CC}	Supply Voltage
17	T2	Testing output pin (not to be used)
18	FSEL	Frequency selector pin
19	TM	Test mode pin (open = normal RUN) (closed to V_{CC} = Test mode)
20	POR	Reset Input for testing (active high)

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, Tamb = 25°C; fosc = 4.332MHz; V_{IN} = 20mVrms unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY						
V_{CC}	Supply Voltage		4.5	5	5.5	V
I_S	Supply Current			9		mA
FILTER						
F_C	Center Frequency		56.5	57	57.5	KHz
BW	3dB Bandwidth		2.5	3	3.5	KHz
G	Gain	f = 57KHz	18	20	22	dB
A	Attenuation	Δf = +4KHz f = 38KHz; V_i = 500mVrms f = 67KHz; V_i = 250mVrms	18 50 35	22 80 50		dB dB dB
ΔPh	Phase non linearity	A (see note1) B (see note1) C (see note1)		0.5 1 2	5 7.5 10	DEG DEG DEG
R_i	Input Impedance		100	160	200	KΩ
S/N	Signal to Noise Ratio	V_i = 3mVrms	30	40		dB
V_i	Input Signal	f = 19KHz; T3 ≤ −40dB (see note2) f = 57KHz (RDS + ARI)			1 50	Vrms mVrms
R_L	Load Impedance	Pin 4	100			KΩ
LIMITER						
RA	Resistance pin 3-4		15	21	28	KΩ
OSCILLATOR						
F_{OSC}	Oscillator Frequency	F_{SEL} = Open (*) F_{SEL} = Closed to V_{CC} (**)		4.332 8.664		MHz MHz
VCLL	Clock Input level LOW				1	V
VCLH	Clock Input Level HIGH		4			V
	Output Amplitude			5		V_{PP}

CHRISTAL TYPE = EURO QUARTZ

(*) FSEL pin has an internal 40KΩ pull down resistor A 4.332MHz QUARTZ must be used (**) A 8.664MHz QUARTZ must be used.

DEMODULATOR

S_{RDS}	RDS Detection Sensitivity		1			mVrms
S_{ARI}	ARI Detection Sensitivity		3			mVrms
T_{lock}	RDS Lockup Time			100		ms
V_{OH}	Output HIGH Voltage	I_L = 0.5mA	4			V
V_{OL}	Output LOW Voltage	I_L = 0.5mA			1	V
f_{RDS}	Data Rate for RDS			1187.5		Hz

Note(1):
The phase non linearity is defined as: $\Delta Ph = | -2\,\phi f2 + \phi f1 + \phi f3 |$
where ϕfx is the input-output phase difference at the frequency fx (x = 1,2,3)

Measure	f1 (KHz)	f2 (KHz)	f3 (KHz)	ΔPh max
A	56.5	57	57.5	<5°
B	56	57	58	<7.5°
C	55.5	57	58.5	<10°

Note(2): The 3th harmonic (57KHz) must be less than -40dB in respect to the input signal plus gain.