TDA7513

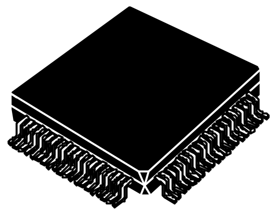
SINGLE-CHIP FM/AM TUNER WITH STEREO DECODER AND AUDIO PROCESSOR

TARGET SPECIFICATION

- AM/FM TUNER FOR CAR-RADIO
- INTEGRATED TUNING PLL
- VARIABLE-BANDWITH FM IF FILTER (ISS)
- FULLY INTEGRATED FM STEREO DECODER
- FULLY INTEGRATED FM NOISE BLANKER
- HIGHLY INTEGRATED AUDIO PROCESSOR

DESCRIPTION

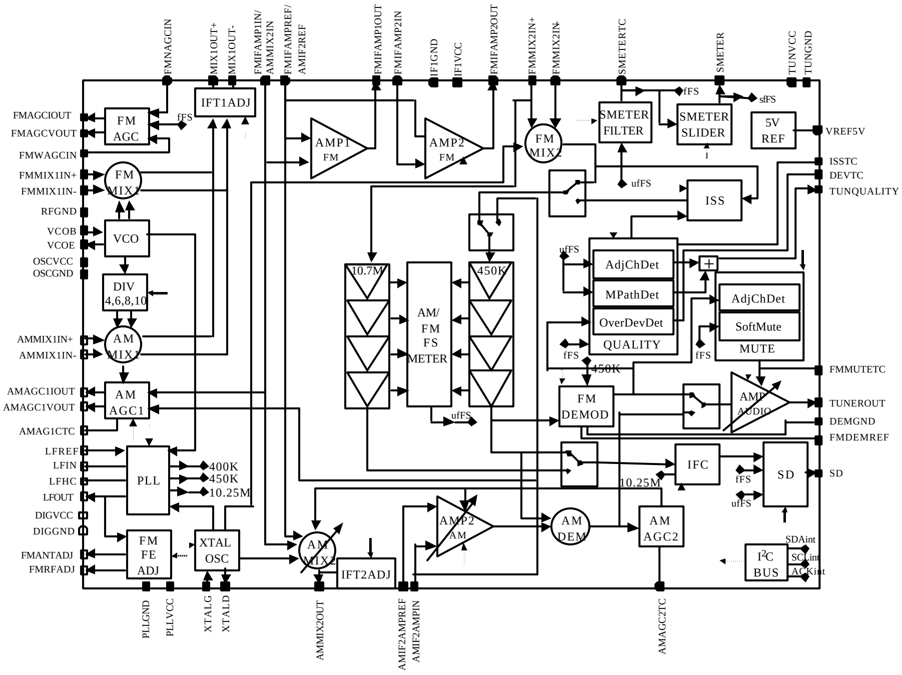
The TDA7513 is the first device for car-radio applications that combines full RF front-end functions with audio-processing capabilities.
As far as FM and AM functions are concerned , the TDA7513 features front-end processing, including the digital tuning PLL, IF processing with demodulation and variable-bandwidth IF filtering (ISS), stop station and quality detection functions, FM stereo decoding by means of a fully-integrated, adjustment-free dedicated PLL and, finally, FM noise blanking. The FM stereo decoder and noise blanker functions are realized entirely without external components.
The audio processor section comprises input selectors for two quasi-differential external sources, volume control, tone control (bass, mid and treble), balance and fading control to drive four output channels. A soft mute function and an RDS mute function are included to handle source change as well as RDS AF search without abrupt changes in the audio level.
Most of the parameters in the front-end section are I^2Cbus -driven and therefore under the control of the car-radio maker. The I^2Cbus allows furthermore the user to realize the full electric alignment of all the external coils, therefore removing the need for hand-made or mechanical adjustments.



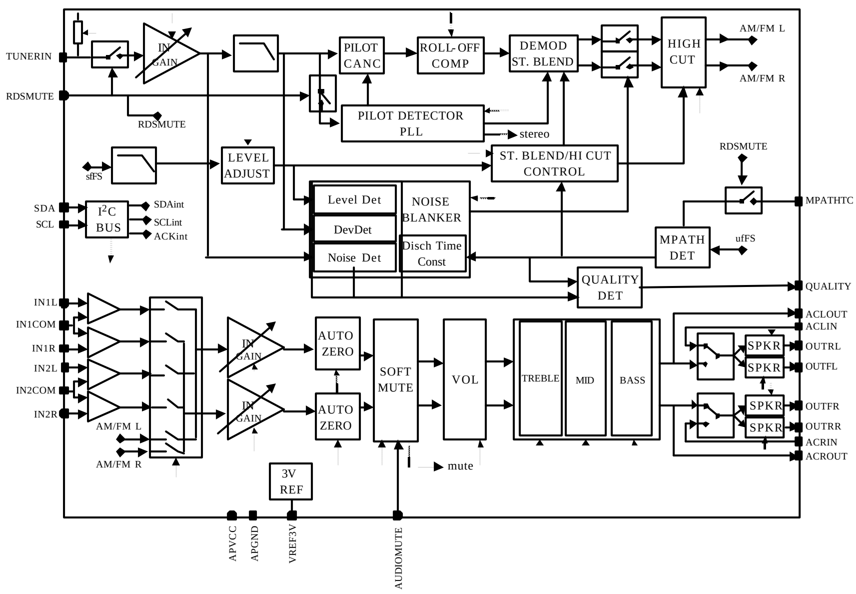
TQFP80

1.0 BLOCK DIAGRAM

1.1 TUNER SECTION



1.2 STEREO DECODER / AUDIO PROCESSOR SECTION



2.0 PIN LIST

#	PIN NAME	PIN FUNCTION
1	VREF5V	5V reference
2	TUNGND	tuner general ground
3	AMMIX1IN1	am mix1 input
4	AMMIX1IN2	am mix1 input
5	AMAGC1TC	am agc1 filter capacitor
6	AMAGC1IOUT	am agc1 current output
7	AMAGC1VOUT	am agc1 voltage output
8	FMMIX1IN1	fm mix1 input
9	RFGND	rf ground
10	FMMIX1IN2	fm mix1 input
11	FMAGCIOUT	fm agc current output
12	FMWAGCIN	fm agc RF input
13	FMAGCVOUT	fm agc voltage output
14	FMANTADJ	fm antenna filter adjustment
15	FMRFANDJ	fm rf filter adjustment
16	OSCGND	vco ground
17	VCOE	am/fm vco emitter
18	VCOB	am/fm vco base
19	OSCVCC	vco supply (8V)
20	LFOUT	PLL loop filter output
21	LFREF	PLL loop filter reference
22	LFIN	PLL loop filter input
23	LFHC	PLL loop filter high-current input
24	PLLVCC	PLL back-end supply
25	PLLGND	PLL back-end ground
26	XTALG	ref osc gate
27	XTALD	ref osc drain
28	DIGVCC	digital dirty supply (8V)
29	DIGGND	digital ground
30	TUNQUALITY	tuner combined output of multipath and adjacent channel detectors
31	ISSTC	ISS time constant
32	DEVTC	deviation detector time constant
33	VREF3V	3V reference
34	APGND	audio processor/stereo decoder ground
35	APVCC	audio processor/stereo decoder supply (8V)
36	OUTRR	audio out
37	OUTRL	audio out
38	OUTFR	audio out
39	OUTFL	audio out
40	ACRIN	ac coupling right input
41	ACROUT	ac coupling right output
42	ACLIN	ac coupling left input
43	ACLOUT	ac coupling left output
44	IN2L	audio in2 left
45	IN2COM	audio in2 common
46	IN2R	audio in2 right
47	IN1R	audio in1 right
48	IN1COM	audio in1 common
49	IN1L	audio in1 left
50	TUNERIN	am audio/fm mpx input
51	TUNEROUT	am audio/fm mpx output

#	PIN NAME	PIN FUNCTION
52	FMMUTETC	fm muting time constant capacitor
53	SDA	I2C bus data
54	SCL	I2C bus clock
55	SD	am/fm station detector output
56	SMETER	am/fm smeter output
57	QUALITY	quality output
58	AUDIOMUTE	audio mute control
59	RDSMUTE	rds mute control
60	MULTIPATHTC	multipath detector time constant
61	FMDEMREF	fm demodulator reference capacitor
62	DEMGND	fm demodulator ground
63	SMETERTC	am/fm smeter filtering capacitor
64	AMIF2AMPREF	am if2 amp feedback capacitor
65	AMIF2AMPIN	am if2 amp input
66	AMAGC2TC	am agc2 filter capacitor
67	AMMIX2OUT	am mix2 single-ended output
68	FMMIX2IN2	fm mix2 input
69	FMMIX2IN1	fm mix2 input
70	FMIFAMP2OUT	fm if1 amp2 output
71	FMIFAMP2IN	fm if1 amp2 input
72	TUNVCC	tuner general supply (8V)
73	FMIFAMPREF	fm if1 amps reference capacitor
74	FMIFAMP1OUT	fm if1 amp1 output
75	FMIFAMP1IN	fm if1 amp1 input
76	FMNAGCIN	fm agc IF input
77	IFGND	if1 ground
78	MIX1OUT2	am/fm mix1 output
79	MIX1OUT1	am/fm mix1 output
80	IFVCC	if1 supply (8V)

3.0 ELECTRICAL PARAMETERS

3.1 FM (V_{CC} = 8V; T_{amb} =25°C; Vsg = 60dBu; fc = 98.1MHz; fdev = 40kHz; fmod = 1kHz unless otherwise specified).

General (audioprocessor all flat and stereo decoder input gain = 4dB)

Symbol	Parameter		Test Condition	Min	Typ	Max	Unit
US	Useable sensitivity		SNR = 40dB		0		dBu
SNR	Signal to Noise ratio				66		dB
LS	Limiting Sensitivity		Soft Mute OFF; @ ΔVout = -3dB		-4		dBu
THD	Total Harmonic Distortion		fdev = 40kHz		0.1	0.3	%
			fdev = 75kHz		0.15	0.5	%
Vout	Audio output level				375		mVrms
ISN	Interstation noise		ΔVout @ RF OFF; Soft Mute OFF		-13		dB
IFCS	IF Counter sensitivity				2	10	dBu
Icc	DC current	OSCVcc			5.7		mA
		PLLVcc			1.9		mA
		DIGVcc			9.8		mA
		TUNVcc			50		mA
		IF1Vcc			13.4		mA
		APVcc			27.3		mA

Mixer1

Symbol	Parameter		Test Condition	Min	Typ	Max	Unit
Gv	conversion gain		from RFT secondary to IFT1 secondary loaded with 330Ω		9		dB
IIP3	3rd order intercept point		referred to RFT secondary				dBu
CIFT1	IFT1 adjustment capacitor	min	Between MIXOUT+ and MIXOUT-		0		pF
		max			8.25		pF
		step			0.55		pF
Rin	input resistance (single ended)		FMMIX1IN+ and FMMIX1IN- w.r.t. gnd		10		Ω

Front-end Adjustment (VRFadj and VANTadj referred to VLFOUT)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Vantadj	min			-40		%
	max			40		%
	step			1.29		%
VRFadj	min			-40		%
	max			40		%
	step			1.29		%

AGC (wide AGC input connected to RFT primary through 10pF and 1KΩ)

Symbol	Parameter		Test Condition	Min	Typ	Max	Unit
WAGCsp	Wide AGC starting point		VRFTprimary @ I(FMAGCOUT) = 5uA		84		dBu
WAGCRin	FMWAGCIN input resistance				125		ohm
NAGCsp	Narrow AGC starting point (max sensitivity)		VRFTprimary @ I(FMAGCOUT) = 5uA; Keyed AGC OFF		95		dBu
KNAGCsp	Keyed narrow AGC starting point (min sensitivity)		VRFTprimary @ I(FMAGCOUT) = 5uA; Keyed AGC ON; V(SMETERTC)<0.9V		109		dBu
NAGCRin	FMNAGCIN input resistance				10		Kohm
KAGCTH high	Smeter for Keyed narrow AGC maximum sensitivity	minimum programming	V(SMETERTC) @ narrow AGC starting point = NAGCsp		0.9		V
		maximum programming			2.5		V

KAGCTH low	Smeter for Keyed narrow AGC minimum sensitivity: minimum programming	V(SMETERTC) @ narrow AGC starting point = KNAGCsp		1.6		V
	maximum programming			3.2		V
Iout	min	AGC OFF			0.1	uA
	max	AGC ON	8			mA
Vout	min	AGC ON		0.1	0.5	V
	max	AGC OFF	Vcc-0.5			V
AGCVRout	FMAGCVOUT output resistance			100		KΩ

IF Amplifier 1 (Input at FMIFAMP1IN, fc = 10.7MHz, no mod) (Output at FMIFAMP1OUT loaded with 330 Ω) (antenna level = FMIFAMP1IN – 31dB)

G	Gain			18		dB
IIP3	3rd order intercept point	referred to FMIFAMP1IN		126		dBu
Rin	input resistance (single-ended)	FMIFAMP1IN w.r.t. gnd		330		Ω
Rout	output resistance			330		Ω

IF Amplifier 2 (Input at FMIFAMP2IN, fc = 10.7MHz, no mod) (Output at FMIFAMP2OUT loaded with 330 Ω) (antenna level = FMIFAMP2IN – 45dB)
Gain MUST BE SET to 14dB for ISS operation.

G	minimum gain	programmable gain		6		dB
				8		dB
				10		dB
	maximum gain			14		dB
IIP3	Input 3rd order intercept point	referred to FMIFAMP2IN, G = 8dB		134		dBu
Rin	input resistance (single-ended)	FMIFAMP2IN to gnd		330		Ω
Rout	output resistance			330		Ω

Field-strength Meter (Input at FMMIX2IN; fc = 10.7MHz, no mod) (antenna level = V67 – 49dB)

FS1	FSmeter1	V(FMMIX2IN+) = 50 dBu		1.4		dBu
FS2	FSmeter2	V(FMMIX2IN+) = 70 dBu		2.7		dBu
FS3	FSmeter3	V(FMMIX2IN+) = 90 dBu		4.4		dBu
FSR	FSmeter filtering resistor	SMETERTC pin		10.7		kΩ
FFSS	Filtered FSmeter Slider: min			0		V
	max			1.5		V
	step			50		mV

MPX output (output at TUNEROUT)

Gc	conversion gain			5.42		mV/kHz
Vaudio	audio level	40kHz		217		mVp

Field-strength Stop Station (Input at FMMIX2IN – fc = 10.7MHz, no mod) (antenna level = V69 – 49dB)

FSSSmin	minimum threshold	Vthr = 0.4V		50		dBu
FSSSmax	maximum threshold	Vthr = 3.4V		78		dBu
FSSSstep	threshold step	ΔVthr = 200mV		3		dB

Soft Mute

SMD	Soft Mute Depth: min			13.4		dB
				16		dB
				19.5		dB
	max			24		dB
MCVlow	Mute control voltage low	V(FMMUTETC) @ No mute attenuation		0.2		V
MCVhigh	Mute control voltage high	V(FMMUTETC) @ Max mute attenuation		2		V

ACMcl	Adjacent channel mute clamp voltage	min	Max V(FMMUTETC) in Adjacent Channel conditions		500		mV
		max			2000		mV
		step			100		mV

ISS Filter (FMIF1AMP1 gain MUST be set to 14dB) *

BW1	Wide bandwidth	Full bandwidth @ -3dB		120		kHz
BW2	Narrow bandwidth			80		kHz
BWwb	Weather Band bandwidth			30		kHz

* if ISS function is not used, SEEK must be set to “ON” in FM

3.2 AM (V_{CC} = 8V; T_{amb} =25°C; Vsg = 74dBu,emf; fc = 999kHz; 30% modulation; fmod = 400Hz unless otherwise specified).

General (with 20pF/65pF dummy antenna; input levels @ SG,emf; output @ audioprocessor output; audioprocessor all flat; stereo decoder input gain = 5.75dB)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
US	Useable sensitivity	SNR = 20dB		26		dBu
SNR	Signal to Noise ratio			56	60	dB
MS	Maximum Sensitivity	@ ΔVout = -10dB		20		dBu
THD	Total Harmonic Distortion	mod =30%, Vsg = 74dBu		0.59		%
		mod =80%, Vsg = 74dBu		1.48		%
		mod =30%, Vsg = 120dBu		1.88		%
		mod =80%, Vsg = 120dBu		3		%
THDLF	THD @ low frequency	mod =30%, Vsg = 74dBu, fmod=100Hz		2		%
Vout	Audio output level			266		mVrms
ISN	Interstation noise level	ΔVout @ RF OFF		-35	-31	dB
IFCS	IF Counter sensitivity		8	10	20	dBu
Icc	DC current OSCVcc			5.6		mA
	PLLVcc			1.9		mA
	DIGVcc			12.1		mA
	TUNVcc			68		mA
	IF1Vcc			7.8		mA
	APVcc			27		mA

Mixer1 (Input at AMMIX1IN+, no mod)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Gv	conversion gain	from AMMIX1IN+to IFT1 secondary loaded with 330 Ω		13		dB
IIP3	Input 3rd order intercept point	referred to AMMIX1IN+		130		dBu
Rin	input resistance (differential)	AMMIX1IN+ w.r.t. AMMIX1IN-		1.2		kΩ
CIFT1	IFT1 adjustment capacitor min	Between MIXOUT+ and MIXOUT-		0		pF
	max			8.25		pF
	step			0.55		pF

AGC1 (Wide AGC input = AM Mixer1 input; Narrow AGC input = AM Mixer2 input; Ultra Narrow AGC input = AM IF2 Amp input; fWAGCin = 999kHz, fNAGCIN = 10.7MHz, fUNAGCin = 450kHz)

WAGCsp	Wide AGC starting point min	AMMIX1IN+ @ I(AMAGC1VOUT) = 1 uA		85		dBu
	max			104		dBu
NAGCsp	NarrowAGC starting point min	AMMIX1IN+ @ I(AMAGC1VOUT) = 1 uA		79		dBu
	max			97		dBu
UNAGCsp	Ultra Narrow AGC starting point min	AMMIX1IN+ @ I(AMAGC1VOUT) = 1 uA		50		dBu
	max			97		dBu
AGC1R	AGC1 filtering resistor	AMAGC1TC pin		100		Kohm
Iout	min	AGC OFF			1	uA
	max	AGC ON	0.4			mA
Vout	min	AGC ON			0.5	V
	max	AGC OFF		3.38		V
AGC1VRout	AMAGC1VOUT output resistance			23		Kohm

Mixer2 (Input at AMMIX2IN, fc = 10.7MHz, no mod)

Gv, max	conversion gain, no AGC	from AMMIX2IN to IFT2 secondary loaded with 2k Ω		15		dB
Gv, min	conversion gain, full AGC	from AMMIX2IN to IFT2 secondary loaded with 2kΩ		-7		dB
IIP3	Input 3rd order intercept point	referred to AMMIX2IN, no AGC		120		dBu

Rin	input resistance		AMMIX2IN w.r.t. ground		330		Ω
CIFT2	IFT2 adjustment capacitor	min	Between AMMIX2OUT and gnd		0		pF
		max			24		pF
		step			1.6		pF

IF2 amplifier (Input at AMIF2AMPIN, fc = 450kHz, no mod)

Gv, max	gain, no AGC	max prog			64.8		dB
					62.8		
					61.7		
					60.2		
					58.3		
					55.8		
		min prog			53.2		
ΔGv	gain decrease in full AGC		w.r.t. Gv, max		-40		dB
Rin	input resistance		AMMIX2IN w.r.t. ground		2		k Ω

AGC2

AGC2R	AGC2 filtering resistor	reception			150		k Ω
		seek			5		k Ω

Audio output (output at TUNEROUT, 2.7k Ω load)

Vaudio	audio level	30%		305		mVrms

Field-strength Meter (Input at AMIF2AMPIN; fc = 450 kHz, no mod) (SG,emf level = V65 – 29dB)

FS1	FSmeter1		V(AMIF2AMPIN) = 50 dBu		0.7		dBu
FS2	FSmeter2		V(AMIF2AMPIN) = 70 dBu		2.1		dBu
FS3	FSmeter3		V(AMIF2AMPIN) = 90 dBu		4.2		dBu
FSR	FSmeter filter resistor	min	SMETERTC pin		16.5		kΩ
		max			75		kΩ
FFSS	Filtered FSmeter Slider	min			0		V
		max			1.5		V
		step			48.4		mV

3.3 OSCILLATORS (V_{CC} = 8V; T_{amb} =25°C)

VCO

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Vvco	Oscillation level	Tuning Voltage = 4V	106		108	dBu
C/N	Carrier to Noise ratio	Δf = 1kHz		85		dBc/Hz

XTAL

Symbol	Parameter		Test Condition	Min	Typ	Max	Unit
Vxtal	Oscillation level		@ XTAL gate		131		dBu
FXTAL	Adjustment frequency range	min	referred to 10.25 MHz centered condition		-4		kHz
		max			+4		kHz
		step			238		Hz

3.3 AUDIO PROCESSOR (VS = 8V; Tamb = 25°C; RL = 10kOhm; all gains = 0dB; f = 1kHz; unless otherwise specified).

Symbol	Parameter		Test Condition	Min.	Typ.	Max.	Unit
INPUT GAIN							
$G_{IN\ MIN}$	Min. Input Gain			-1	0	1	dB
$G_{IN\ MAX}$	Max. Input Gain			13	15	17	dB
G_{STEP}	Step Resolution			0.5	1	1.5	dB
QUASI DIFFERENTIAL STEREO INPUT 1&2							
R_{in}	Input Resistance		Any input pin to gnd	70	100	130	kΩ
CMRR	Common Mode Rejection Ratio		V_{CM} = $1V_{RMS}$ @ 1kHz	45	70		dB
			V_{CM} = $1V_{RMS}$ @ 10kHz	45	60		dB
VOLUME CONTROL							
G_{MAX}	Max Gain			13	15	17	dB
A_{STEP}	Step Resolution			0.5	1	1.5	dB
E_A	Attenuation Set Error		G = -20 to 20dB	-1.25	0	1.25	dB
			G = -60 to 20dB	-4	0	3	dB
E_T	Tracking Error					2	dB
V_{DC}	DC Steps		Adjacent Attenuation Steps				mV
			From 0dB to G_{MIN}				mV
SOFT MUTE/AFS							
A_{MUTE}	Mute Attenuation			80	100		dB
T_D	Delay Time	T1			0.48		ms
		T2			0.96		ms
		T3			20.2		ms
		T4			40.4		ms
$V_{TH\ low}$	Low Threshold for SM-/AFS- Pin [1]					1	V
$V_{TH\ high}$	High Threshold for SM-/AFS-Pin			4			V
BASS CONTROL							
C_{RANGE}	Control Range			±13	±15	±17	dB
A_{STEP}	Step Resolution			0.5	1	1.5	dB
f_C	Center Frequency		f_{C1}	54	60	66	Hz
			f_{C2}	63	70	77	Hz
			f_{C3}	72	80	88	Hz
			f_{C4}	90	100 (150) [2]	110	Hz
Q_{BASS}	Quality Factor		Q_1	0.9	1	1.1	
			Q_2	1.1	1.25	1.4	
			Q_3	1.3	1.5	1.7	
			Q_4	1.8	2	2.2	
DC_{GAIN}	Bass-Dc-Gain		DC = off	-1	0	1	dB
			DC = on	3.5	4.4	5.5	dB
MID CONTROL							
C_{RANGE}	Control Range			±13	±15	±17	dB
A_{STEP}	Step Resolution			0.5	1	1.5	dB
f_C	Center Frequency		f_{C1}	450	500	550	Hz
			f_{C2}	0.9	1	1.1	kHz
			f_{C3}	1.35	1.5	1.65	kHz
			f_{C4}	1.8	2	2.2	kHz
Q_{BASS}	Quality Factor		Q_1	0.9	1	1.1	
			Q_2	1.8	2	2.2	
TREBLE CONTROL							
C_{RANGE}	Control Range			±13	±15	±17	dB
A_{STEP}	Step Resolution			0.5	1	1.5	dB
f_C	Center Frequency		f_{C1}	8	10	12	kHz
			f_{C2}	10	12.5	15	kHz
			f_{C3}	12	15	18	kHz

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
		f_{C4}	14	17.5	21	kHz
SPEAKER ATTENUATORS						
R_{IN}	Input Impedance		17.5	25	32.5	kΩ
G_{MAX} A_{MAX}	Max Gain Max Attenuation		13 -70	15 -79	17	dB dB
A_{STEP}	Step Resolution		0.5	1	1.5	dB
A_{MUTE}	Output Mute Attenuation		80	90		dB
E_E	Attenuation Set Error				±2	dB
V_{DC}	DC Steps	Adjacent Attenuation Steps				mV
AUDIO OUTPUTS						
V_{CLIP}	Clipping Level	THD = 0.3%	2.2	2.6		V_{RMS}
R_L	Output Load Resistance		2			kΩ
C_L R_{OUT}	Output Load Capacitance Output Impedance			30	10 120	nF Ω
V_{DC}	DC Voltage Level			3.9		V
GENERAL						
Gqd	Gain (QDin)	Quasi-differential Input		0.5		dB
Gstd	Gain (Tuner)	Tuner Input (STD InGain=4dB)		7.5		dB
e_{NO}	Output Noise (QDin)	BW = 20 Hz to 20 kHz output muted; all flat			15	µV
		BW = 20 Hz to 20 kHz all gain = 0dB		20		µV
S/N	Signal to Noise Ratio (QDin)	all gain = 0dB flat; V_O = 2V_{RMS}		100		dB
		bass treble at 12dB; A-weighted; V_O = 2.6V_{RMS}		96		dB
d	Distortion (QDin)	V_{IN} = 1V_{RMS}; all stages 0dB		0.012	0.1	%
		V_{IN} = 1V_{RMS}; Bass & Treble = 12dB		0.05	0.1	%
S_C	Channel separation Left/Right (QDin)		80			dB
E_T	Total Tracking Error	A_V = 0 to -20dB	-1	0	1	dB
		A_V = -20 to -60dB	-2	0	2	dB
BUS INPUTS						
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage		2.5			V
I_{IN}	Input Current	V_{IN} = 0.4V	-5		5	µA
V_O	Output Voltage SDA Acknowledge	I_O = 1.6mA			0.4	V

1) The SM pin is active low (Mute = 0)
2) See note in Programming Part

3.4 STEREO DECODER (Vcc = 8V; deemphasis time constant = 50µs, VMPX = 305mVrms (75kHz deviation), fm= 1kHz, Gv = 4dB, Tamb = 27°C; unless otherwise specified).

Symbol	Parameter		Test Condition	Min.	Typ.	Max.	Unit
R_{in}	Input Resistance	FM		70	100	130	kΩ
		AM		1.4	2	2.6	kΩ
G_V	Stereo decoder input gain	min			0.5		dB
					2.25		dB
					4.0		dB
		max			5.75		dB
SVRR	Supply Voltage Ripple Rejection		V_{ripple} = 100mV; f = 1KHz	35	60		dB
α	Max. channel Separation			30	45		dB
THD	Total Harmonic Distortion				0.02	0.3	%
(S+N)/N	Signal plus Noise to Noise Ratio		A-weighted, S = $2V_{rms}$ @ APout	80	91		dB
MONO/STEREO-SWITCH							
V_{PTHST1}	Pilot Threshold Voltage		for Stereo, PTH = 1		15		mV
V_{PTHST0}	Pilot Threshold Voltage		for Stereo, PTH = 0		25		mV
V_{PTHMO1}	Pilot Threshold Voltage		for Mono, PTH = 1		12		mV
V_{PTHMOO}	Pilot Threshold Voltage		for Mono, PTH = 0		19		mV
PLL							
Δf/f	Lock Range			-6		+6	%
f0	Center frequency range	min	VCO Vtuning fixed to reference voltage		328		kHz
		max			619		kHz
		step			9.4		kHz
PILmax	Maximum input pilot voltage		@TUNERIN	276			mV
DEEMPHASIS and HIGHCUT							
τ_{HC50}	Deemphasis Time Constant		Bit 7, Subadr, 10 = 0, $V_{LEVEL} >> V_{HCH}$	25	50	75	µs
τ_{HC75}	Deemphasis Time Constant		Bit 7, Subadr, 10 = 1, $V_{LEVEL} >> V_{HCH}$	50	75	100	µs
τ_{HC50}	Highcut Time Constant		Bit 7, Subadr, 10 = 0, $V_{LEVEL} >> V_{HCL}$	100	150	200	µs
τ_{HC75}	Highcut Time Constant		Bit 7, Subadr, 10 = 1, $V_{LEVEL} >> V_{HCL}$	150	225	300	µs
STEREOBLEND - and HIGHCUT-CONTROL							
REF5V	Internal Reference Voltage			4.7	5	5.3	V
L_{Gmin}	Min. LEVEL Gain			-1	0	1	dB
L_{Gmax}	Max. LEVEL Gain			8	10	12	dB
L_{Gstep}	LEVEL Gain Step Resolution			0.3	0.67	1	dB
$VSBL_{min}$	Min. Voltage for Mono			25	29	33	%REF5V
$VSBL_{max}$	Max. Voltage for Mono			54	58	62	%REF5V
$VSBL_{step}$	Step Resolution			2.2	4.2	6.2	%REF5V
$VHCH_{min}$	Min. Voltage for NO Highcut			38	42	46	%REF5V
$VHCH_{max}$	Max. Voltage for NO Highcut			62	66	70	%REF5V
$VHCH_{step}$	Step Resolution			5	8.4	12	%REF5V
$VHCL_{min}$	Min. Voltage for FULL Highcut			12	17	22	%VHCH
$VHCL_{max}$	Max. Voltage for FULL Highcut			28	33	38	%VHCH
$VHCL_{step}$	Step Resolution			2.2	4.2	6.2	%VHCH
Carrier and harmonic suppression at the output							
α19	Pilot Signal f = 19KHz			40	50		dB
α38	Subcarrier f = 38KHz					75	dB
α57	Subcarrier f = 57KHz					62	dB
α76	Subcarrier f = 76KHz					90	dB

3.5 NOISE BLANKER

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V_{TR}	Trigger Threshold 0) 1)	meas. with V_{PEAK} =	NBT = 111	(c)	30	(c)	mV_{OP}

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		0.9V	NBT = 110	(c)	35	(c)	mV_{OP}
			NBT = 101	(c)	40	(c)	mV_{OP}
			NBT = 100	(c)	45	(c)	mV_{OP}
			NBT = 011	(c)	50	(c)	mV_{OP}
			NBT = 010	(c)	55	(c)	mV_{OP}
			NBT = 001	(c)	60	(c)	mV_{OP}
			NBT = 000	(c)	65	(c)	mV_{OP}
$V_{TRNOISE}$	Noise Controlled Trigger threshold 2)	meas. with V_{PEAK} = 1.5V	NCT = 00	(c)	260	(c)	mV_{OP}
			NCT = 01	(c)	220	(c)	mV_{OP}
			NCT = 10	(c)	180	(c)	mV_{OP}
			NCT = 11	(c)	140	(c)	mV_{OP}
V_{RECT}	Rectifier Voltage	V_{MPX} = 0mV	NRD 6) = 00	0.5	0.9	1.3	V
		V_{MPX} = 50mV; f = 150KHz		1.5	1.7	2.1	V
		V_{MPX} = 200mV; f = 150KHz		2.2	2.5	2.9	V
$V_{RECTDEV}$	deviation dependent rectifier Voltage 3)	meas. with V_{MPX} = 800mV (75KHz dev.)	OVD = 11	0.5	0.9	1.3	V_{OP}
			OVD = 10	0.9	1.2	1.5	V_{OP}
			OVD = 01	1.7	2	2.3	V_{OP}
			OVD = 00	2.5	2.8	3.1	V_{OP}
$V_{RECT FS}$	Fieldstrength Controlled Rectifier Voltage 4)	Rectifier Voltage 4) V_{MPX} = 0mV V_{LEVEL} << V_{SBL} (fully mono)	FSC = 11	0.5	0.9	1.3	V
			FSC = 10	0.9	1.4	1.5	V
			FSC = 01	1.7	1.9	2.3	V
			FSC = 00	2.1	2.4	3.1	V
T_S	Suppression Pulse Duration 5)	Signal HOLDN in Testmode	BLT = 00		38		µs
			BLT = 10		32		µs
			BLT = 01		25.5		µs
			BLT = 00		22		µs
$V_{RECTADJ}$	Noise Rectifier discharge adjustment 6)	Signal PEAK in Testmode	NRD = 00 6)	(c)	0.3	(c)	V/ms
			NRD = 01 6)	(c)	0.8	(c)	V/ms
			NRD = 10 6)	(c)	1.3	(c)	V/ms
			NRD = 11 6)	(c)	2	(c)	V/ms
SR_{PEAK}	Noise Rectifier Charge	Signal PEAK in Testmode	PCH = 0 7)	(c)	10	(c)	mV/µs
			PCH = 1 7)	(c)	20	(c)	mV/µs
V_{ADJMP}	Noise Rectifier adjustment through Multipath 8)	Signal PEAK in Testmode	MPNB = 00 8)	(c)	0.3	(c)	V/ms
			MPNB = 00 8)	(c)	0.5	(c)	V/ms
			MPNB = 00 8)	(c)	0.7	(c)	V/ms
			MPNB = 00 8)	(c)	0.9	(c)	V/ms

(c) = by design/characterization functionally guaranteed through dedicated test mode structure
0) All Thresholds are measured using a pulse with T_R = 2µs, T_{HIGH} = 2µs and T_F = 10µs. The repetition rate must not increase the PEAK voltage.
1) NBT represents the Noiseblanker Byte bits D_2, D_0 for the noise blanker trigger threshold
2) NAT represents the Noiseblanker Byte bit pair D_4, D_3 for the noise controlled triggeradjustment
3) OVD represents the Noiseblanker Byte bit pair D_7, D_6 for the over deviation detector
4) FSC represents the Fieldstrength Byte bit pair D_1, D_0 for the fieldstrength control
5) BLT represents the Speaker RR Byte bit pair D_7, D_6 for the blanktime adjustment
6) NRD represents the Configuration-Byte bit pair D_1, D_0 for the noise rectifier discharge-adjustment
7) PCH represents the Stereodecoder-Byte bit D_5 for the noise rectifier charge-current adjustment
8) MPNB represents the HighCut-Byte bit D_7 and the Fieldstrength-Byte D_7 for the noise rectifier multipath adjustment

3.6 MULTIPATH AND QUALITY DETECTORS

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
f_{CMP}	Center Frequency of Multipath-Bandpass	Stereodecoder locked on Pilottone			19		kHz
G_{BPMP}	Bandpass Gain	bits D_2, D_1 configuration byte = 00			6		dB
		bits D_2, D_1 configuration byte = 10			12		dB
		bits D_2, D_1 configuration byte = 01			16		dB
		bits D_2, D_1 configuration byte = 11			18		dB
G_{RECTMP}	Rectifier Gain	bits D_7, D_6 configuration byte = 00			7.6		dB
		bits D_7, D_6 configuration byte = 01			4.6		dB
		bits D_7, D_6 configuration byte = 10			0		dB
		bits D_7, D_6 configuration byte = 11			off		
I_{CHMP}	Rectifier Charge Current	bit D_5 configuration byte = 0			0.5		µA
		bit D_5 configuration byte = 1			1		µA
I_{DISMP}	Rectifier Discharge Current			0.5	1	1.5	mA
A	Multipath Influence Factor	Addr. 12 / Bit 5+6	00		0.7		dB
			01		0.85		dB
			10		1		dB
			11		1.15		dB
B	Noise Influence Factor	Addr. 16 / Bit 1+2	00		15		dB
			01		12		dB
			10		9		dB
			11		6		dB

4.0 FUNCTIONAL DESCRIPTION

4.1 FM Section

Mixer1, AGC and 1st IF

Mixer1 is a wide dynamic range stage with low noise and large input signal performance. The mixer1 tank center frequency can be adjusted by software (IF1T). The AGC operates on different sensitivities and bandwidths (FMAGC) in order to improve the input sensitivity and dynamic range (keyed AGC). The output signals of AGC are controlled voltage and current for preamplifier and prestage P-I-N diode attenuator (see Figure 5). Two 10.7MHz amplifiers (IFG1 – fixed gain - and IFG2 - programmable) correct the IF ceramic insertion loss.

Mixer2, Limiter and Demodulator

In this 2nd mixer stage the first 10.7MHz IF is converted into the second 450kHz IF. A multi-stage limiter generates signals for the complete integrated demodulator without external tank. MPX output DC offset compensation is possible via software.

Quality Detection and ISS (see Figure 3)

Fieldstrength

Parallel to the mixer2 input a 10.7MHz limiter generates a signal for the digital IF counter and a fieldstrength output signal. This internal unfiltered fieldstrength is used for adjacent channel and multipath detection. The behaviour of this output signal can be corrected for DC offset (SL). The internally generated unfiltered fieldstrength is filtered at pin #SMETERTC and used for softmute function, FM AGC keying and generation of ISS filter switching signal for weak input level (sm).

Adjacent Channel Detector

The input of the adjacent channel detector is AC coupled to the internal unfiltered fieldstrength. A programmable and configurable highpass or bandpass filter (ACF) and amplifier (ACG) followed by a rectifier measure the adjacent channel content. This voltage is compared with an adjustable threshold (ACWTH, ACNTH) comparator (comparator1). The output signal of this comparator generates a DC level at PIN15 with a programmable time constant. Time constant control (TISS) for the adjacent channel is made by linearly charging and discharging an external capacitor following. The charge current is fixed and the discharge current is controlled by I^2C bus. This level produces digital signals (ac, ac+) after comparing by the following comparator4. The adjacent channel information after filtering and rectification is available as analog output on pin #TUNQUALITY (the gain can be selected via I^2C bus) in combination with multipath content information. It is possible to enable adjacent channel content information output only via I^2C bus control.

Multipath Detector

The input of the multipath detector is AC coupled to the internal unfiltered fieldstrength. A programmable band-pass filter (MPF) and amplifier (MPG) followed by a rectifier measures the multipath content. This voltage is compared with an adjustable threshold (MPTH) comparator (comparator2). The output signal of this comparator2 is used to disable the adjacent channel detector control of the ISS filter in case of strong multipath, which would otherwise result in bandwidth reduction because of the multipath-induced high-frequency content of the fieldstrength signal. The multipath detector influence on the adjacent channel detector is selectable by I^2C bus (MPOFF). The multipath information after filtering and rectification is available as analog output on pin #TUNQUALITY (the gain can be selected via I^2C bus) in combination with the adjacent channel content information. It is possible to enable multipath content information output only via I^2C bus control.

450kHz IF Narrow Bandpass Filter (ISS filter)

The device features an additional automatically selectable IF narrow bandpass filter for suppression noise and adjacent channel signals. This narrow filter has three switchable bandwidth positions: narrow range (80kHz), mid range (120kHz) and weather band (30kHz). WHen the ISS filter is not inserted the IF bandwidth (wide range) is defined only by the ceramic filter chain. The filter is switched in after mixer2 before the 450kHz limiter stage. The centre frequency can be finely adjusted (AISS) by software.

Deviation Detector

In order to avoid excessive audio distortion the narrow ISS filter is switched OFF when overdeviation of the incoming signal is detected. The demodulator output signal is low-pass filtered and rectified to generate a DC level in an external capacitor through a software-controlled current (TDEV). This level is compared with a programmable threshold (DWTH, DTH) comparator (comparator3) to generate two digital signals (dev, dev+).

ISS Switch Logic

All digital signals coming from adjacent channel detector, deviation detector and softmute are combined in a decision matrix to generate the control signals for the ISS filter switch. The IF bandpass switch mode can be also controlled by software (ISSON, ISS30, ISS80, ISSCTL). The switch-on of the IF bandpass can be further controlled from the outside by manipulation of the voltage at pin #ISSTC. Two application modes are available (APPM). The conditions are described in table 1.

Soft Mute Control

The external fieldstrength signal at pin #SMETERTC is the reference for MPX mute control. The start point and mute depth are programmable over a wide range. The time constant is defined by the external capacitor connected to pin #FMMUTETC.
Additionally adjacent channel mute function is supported. A software-configurable highpass / bandpass filter centered at about 100kHz followed by an amplifier and a peak rectifier generates adjacent noise information starting from the MPX output; the information is acted upon with the same time constant as the softmute by the MPX muting circuit. The adjacent channel mute starting point, slope and depth are I^2C bus programmable.

Station Detector and Seek Stop

A station detection function is provided for easy seek stop operation. The unfiltered fieldstrength signal is compared with a programmable threshold and the result (logic ‘1’ if the current station strength is higher than the threshold) is combined by an AND gate with the IF counter output (logic ‘1’ if the current channel is centered within a programmable window around the desired frequency). The result is available on pin #SD for direct connection to the microprocessor. Channel quality assessment for RDS Alternate Frequency operation makes use of the SD signal in conjunction with analog information on adjacent channel and multipath content on pin #TUNQUALITY and channel noise (furtherly combined with multipath content information) on pin #QUALITY.

4.2 AM Section

The upconversion mixer1 is combined with a gain control circuit 1 sensing three input signals: ultra-narrow band information (from the IF2 amplifier input – pin #AMIF2AMPIN), narrow-band information (from the mixer2 input – pin #AMMIX2IN) and wide band information (from the mixer1 input – pins #AMMIX1IN+ and #AMMIX1IN-). This gain control circuit generates two output signals: a current for P-I-N diode attenuation and a voltage for the external preamplifier cascode upper base. It is possible to put in a separate narrow bandpass filter before mixer2 at PIN 58. The intervention point for first AGC on all three bands is programmable by software.
The oscillator frequency for mixer1 is generated by dividing the FM VCO frequency (AMD) by 6, 8 and 10 (6 for Japan applications, 8 for Eastern European applications, 10 for Western European and North American operation).
In mixer2 the IF1 is downconverted into the 450kHz IF2. The gain of mixer2 is reduced by the 2^{nd} AGC after the gain of the subsequent IF2 amplifier has been reduced by 30dB. The mixer2 tank center frequency is software-adjustable (IF2T).
After channel selection is done by the ceramic filter, a 450kHz amplifier with a gain control is included. The gain is controlled by the AGC2 loop over a 30dB range; the full gain with no AGC applied is programmable.
The AM demodulation is made by multiplication of the IF2 amplifier output by the amplified and limited signal coming from the IF2 amplifier input, thus making the demodulation process inherently linear.
The demodulated audio signal is low-passed by the capacitor at pin #AMAGC2TC to produce the DC AGC2 voltage. The low-pass time constant is switchable by a ratio of 30 in order to reduce the settling time of the AGC2 in ‘seek’ mode (AMSEEK).
The FM 450kHz limiter is used to generate the square wave needed by the AM demodulator, a fieldstrength indication and to feed the AM IF

counter. The fieldstrength information is generated mainly from the narrow-band signal at the input of the IF2 amplifier; since the dynamic range at that input is limited by the AGC2 action, a fieldstrength extension is made adding the contribution of the signal at the input of mixer2. Since the bandwidth there is very large, though, the latter contribution is enabled only if the strength of the narrow-band signal is higher than an internally defined threshold. The fieldstrength signal must be low-passed to remove audio content and this is done by use of the capacitor at pin #SMETERTC with an I^2C bus programmable internal resistor. The value of the capacitor is determined for correct FM operation; the value of the internal resistor for AM is selectable in order to make the AM time constant suitable for AM operation.
A station detection function is provided for easy seek stop operation. The fieldstrength signal is compared with a programmable threshold and the result (logic '1' if the current station strength is higher than the threshold) is combined by an AND gate with the IF counter output (logic '1' if the current channel is centered within a programmable window around the desired frequency). The result is available on pin #SD for direct connection to the microprocessor.

4.3 PLL and IF Counter Section

The IC contains a frequency synthesizer and a loop filter for the radio tuning system. Only one VCO is required to build a complete PLL system for FM and AM upconversion. For auto search stop operation an IF counter system is available.

PLL Frequency Synthesizer Block
The counter works in a two stages configuration. The first stage is a swallow counter with a two-modulus (32/33) precounter. The second stage is an 11-bit programmable counter. The circuit receives the scaling factors for the programmable counters and the values of the reference frequency via I^2C bus. The reference frequency is generated by an adjustable internal (XTAL) oscillator followed by the reference divider. The reference and step-frequencies are independently selectable (RC, PC). The phase-frequency detector outputs switches the programmable current source. The loop filter integrates the latter to a DC voltage. The current source values is programmable with 6 bits received via I^2C bus (A, B, CURRH, LPF). To minimize the noise induced by the digital part of the system, a special guard area is implemented. The loop gain can be adjusted for different conditions by setting the current values of the chargepump generator.

Frequency Generation for Phase Comparison
The VCO signal is fed to a two-modulus counter (32/33) prescaler, which is controlled by a 5-bit divider (A). A 5-bit register (PC0 to PC4) controls this divider. The output of the prescaler is connected to an 11-bit divider (B), controlled by an 11-bit PC register (PC5 to PC15).
The following expressions relate the divider output frequency (f_{SYN}, forced by the loop to equal the reference frequency at the phase comparator input f_{REF}) to the VCO frequency (f_{VCO}) and to the crystal oscillator frequency (f_{XTAL}):
$f_{XTAL} = (R+1) \times f_{REF}$
$f_{VCO} = [33 \times A + (B + 1 - A) \times 32] \times f_{REF}$
$f_{VCO} = (32 \times B + A + 32) \times f_{REF}$
Important: For correct operation: A 32; B A

Three State Phase Comparator
The phase comparator generates a phase error signal according to phase difference between f_{SYN} and f_{REF}. This phase error signal drives the charge pump current generator.

Charge Pump Current Generator
This system generates correction current pulses with a polarity and a duration dictated by the phase error signal. The current absolute values are programmable through register A for high current and register B for low current.

Inlock Detector
The charge pump operates in high current mode when the phase difference between between f_{SYN} and f_{REF} is high. The switch back to low current mode can be done either automatically as a function of the inlock detector output (setting bit LDENA to "1") or via software.
After reaching a phase difference equivalent to 10-40 ns (programmable) and a delay multiple of $1/f_{REF}$, the chargepump is forced in low current mode. A new PLL divider programming by I^2C bus will switch the chargepump into high current mode.

A few programmable phase errors (D0, D1) are available for inlock detection. The count of detected inlock informations to release the inlock signal is adjustable (D2, D3), to avoid switching to low current during a frequency jump.

Low Noise CMOS Op-amp

An internal voltage divider at pin #LFREF is connected to the positive input of the low noise op-amp. The charge pump output is connected to the negative input. This internal amplifier in cooperation with external components provides the active loop filter. Only one loop filter connection is provided because the same reference frequency is used for both AM and FM operation. The pin #LFHC is connected in such a way as to partially shunt the loop filter in order to decrease the time constant of the filter itself during jumps with high current mode activated.

IF Counter Block

The input signal for FM and AM has the same structure although FM IF is measured at IF1 (10.7MHz) and AM IF is measured at IF2 (450kHz). The degree of integration is adjustable to up to eight different measuring cycle times. The tolerance of the accepted count value is adjustable to reach the optimum compromise between search speed and evaluation precision.

T center frequency of the measured count value is adjustable to fit the IF-filter tolerance.

The IF-Counter Mode

The IF counter works in 2 modes controlled by the IFCM register.

Sampling Timer

A 14-bit programmable (IRC) sampling timer generates the gate signal for the main counter. In FM mode a 6.25kHz frequency reference is generated for this purpose, whereas in AM mode this reference becomes 1kHz. These reference frequencies are further divided to generate the measurement time windows (160us – 320us ... 20.48ms for FM, 1ms – 2ms … 128ms for AM).

Intermediate Frequency Main Counter

This counter is a 11 - 21-bit synchronous autoreload down counter. Five bits (CF) are programmable to allow the adjustment to the peak of the IF-filter response. The counter length is automatically adjusted to the chosen sampling time and counter mode (FM, AM). The IF counter is also used to automatically perform the stereo decoder 456kHz VCO frequency adjustment.

At the start the counter will be loaded with a value equivalent to the expected number of zero-crossing in the sampling time window ($t_{Sample} \times f_{IF}$). If the correct frequency is applied to the IF counter input, at the end of the sampling time the main counter will have either a 0h state or a 1FFFFFh state stored. A deviation from the expected IF will result in a difference of the counter final state from either of these values. The counter final state is then compared to either 0h or 1FFFFFh minus a number of LSB's determined by the acceptable frequency window programming (EW). If the comparison result is good the IF counter output changes from LOW to HIGH and is made available outside at the pin #SD (after a NAND operation with the signal strength evaluation circuit). The following relationships apply:

$t_{TIM} = (IRC + 1) / f_{OSC}$

$t_{CNT} = (CF + 1697) / f_{IF}$ (FM mode)

$t_{CNT} = (CF + 448) / f_{IF}$ (AM mode)

where

t_{TIM} = IF timer cycle time (sampling time)

t_{CNT} = IF counter cycle time

Counting succesful:

$t_{CNT} - t_{ERR}$ t_{TIM} $t_{CNT} + t_{ERR}$

Count failed:

$t_{TIM} > t_{CNT} + t_{ERR}$

$t_{TIM} < t_{CNT} - t_{ERR}$

where

t_{ERR} = discrimination window (controlled by the EW registers)

The IF counter can be started only by inlock information from the PLL, and it is enabled by software (IFENA).

Adjustment of the Measurement Time and Frequency window

The measurement precision is adjustable by controlling the width of the frequency discrimination window through control registers EW0 to EW2. The center frequency of the discrimination window is adjustable by the control register CF0 to CF4. The measurement time per cycle is adjustable by setting the registers IFS0 - IFS2.

4.4 AUDIO PROCESSOR

Input Multiplexer
CD quasi differential 1
CD quasi differential 2
Stereodecoder input (for both FM and AM signals).

Input stages
The quasi-differential input stages (see figure 4) have been designed to cope with some CD players in the market having a significant high source impedance which affects strongly the common-mode rejection of “normal” differential input stages. The additional buffer of the CD input avoids this drawback and offers the full common-mode rejection even with those CD players. The quasi-differential input can also be used with normal stereo single-ended output signal sources such as TAPEOUT.

AutoZero
In order to reduce the number of pins there is no AC coupling between the In-Gain and the following stage, so that in theory any offset generated by or before the In-Gain stage would be transferred or even amplified to the output. To avoid this undesired situation a special offset cancellation stage called AutoZero is implemented. This stage is located before the Volume block to eliminate all offsets generated by the Stereodecoder, the Input Stage and the In-Gain stage (please note that externally generated offsets, e.g. those generated because of leakage current into the coupling capacitors, are not cancelled).
The auto-zeroing is started every time the APSD data byte 0 is selected and takes a maximum time of 0.6ms. The rationale behind this choice is that the APSD byte encodes the signal source selection, and auto-zero ought to be performed every time a new source is selected. To avoid audible clicks the audioprocessor is muted before the volume stage during this time.

AutoZero Remain
In some cases, for example if the uP is executing a refresh cycle of the I^2C bus programming, it is not necessary to start a new AutoZero action because no new source is selected and an undesired mute would appear at the outputs. For such applications the device can be switched in the "AutoZero Remain mode" (Bit 6 of the APSD subaddress byte). If this bit is set to high, the APSD data byte 0 can be loaded without invoking the AutoZero and the old adjustment value remains.

Softmute
The digitally controlled softmute stage allows signal muting and unmuting with a I^2C bus programmable slope. The mute process can either be activated by pin #AUDIOMUTE or I^2C bus. The slope is realized in a special S-shaped curve so as to slowly mute in the critical regions (see figure 5). For timing purposes the Bit 3 of the I^2C bus output register is set to 1 from the start of muting until the end of unmuting.

BASS
There are four parameters programmable in the bass filter stage: (see figs 6, 7, 8, 9):
Attenuation
Figure 6 shows the attenuation as a function of frequency at a center frequency at a center frequency of 80Hz.
Center Frequency
Figure 7 shows the four possible center frequencies: 60,70,80 and 100Hz.
Quality Factors
Figure 8 shows the four possible quality factors: 1, 1.25, 1.5 and 2.

DC Mode
In this mode the DC gain is increased by 5.1dB. In addition the programmed center frequency and quality factor is decreased by 25%: this can be used to realize different center frequencies or quality factors with respect to the values listed in the “BASS” section.

MID
There are 3 parameters programmable in the mid filter stage (see figs. 10, 11 & 12):
Attenuation
Figure 10 shows the attenuation as a function of frequency at a center frequency of 1kHz.
Center Frequency

Figure 11 shows the four possible center frequencies: 500Hz, 1kHz, 1.5kHz and 2kHz.

Quality Factor

Figure 12 shows the two possible quality factors (1 and 2) at a center frequency of 1kHz.

TREBLE

There are two parameters programmable in the treble filter stage (see figs 13, 14):

Attenuation

Figure 13 shows the attenuation as a function of frequency at a center frequency of 17.5kHz.

Center Frequency

Figure 14 shows the four possible Center Frequencies: 10, 12.5, 15 and 17.5kHz.

AC Coupling

In some applications additional signal manipulations are desired such as surround-sound processing or more extensive band equalizing. For this purpose a AC-Coupling is placed before the Speaker-attenuators, which can be activated or internally shorted by Bit7 in the APSD data byte 0. The input impedance of the AC Inputs is 25k Ω. The external AC coupling is advised for those applications where very low-level “pop” performance is a must.

Speaker Attenuator

The speaker attenuators have exactly the same structure and range as the Volume stage.

4.5 STEREODECODER

The stereodecoder part of the present device (see Fig. 15) contains all functions necessary to demodulate the MPX signal such as pilot tone-dependent MONO/STEREO switch as well as "stereoblend" and "highcut" functions.

Stereodecoder Mute

The device has a fast and easy-to-control RDS mute function meant for “freezing” the stereo decoder status during the RDS AF check time period. When this function is invoked three effects take place:

1) the stereo decoder input impedance changes to infinity (condition known as high-ohmic input); this prevents the decoupling capacitor between the pins #TUNER_OUT (tuner output) and #TUNER_IN (stereo decoder input) to be discharged by a channel with a potentially different DC output for the duration of the AF check;
2) the stereo decoder PLL pilot detector is held at the current value;
3) the external capacitor of the multipath detector used inside the stereo decoder for quality control is disconnected from the dection circuit in order to make quality checking the AF faster.

The RDS mute is activated from pin #RDSMUTE in AND with Bit 0 of APSD data byte 9.

Stereo Decoder Input stage, Ingain + Infilter

The stereo decoder is crossed by both the FM and the AM signal: the input impedance of the pin #TUNER_IN is different between the two modes in order to allow the same external coupling components between #TUNER_OUT and #TUNER_IN to realize different filtering functions. Whilst the input impedence in FM is 100kΩ, in AM the input impedance is decreased to 2k Ω: this allows the realization of typical high-pass filters with a corner frequency of 70Hz for AM and less than 5Hz for FM. The low-pass section of the typical AM transfer function is realized by use of the internal FM High-Cut filter.

The Ingain stage allows to adjust the MPX signal to a magnitude of about 1Vrms internally which is the recommended value. The 4th order input filter has a corner frequency of 80kHz and is used to attenuate spikes and nose and acts as an anti aliasing filter for the following switch capacitor filters.

Demodulator

In the demodulator block the left and the right channel are separated from the MPX signal. In this stage the 19 kHz pilot tone is cancelled.

To reach a good channel separation the device offers an I^2C bus programmable roll-off adjustment which is able to finely compensate for the low-pass behaviour of the tuner section. An adjustment to better than 40dB channel separation is possible.

The bits for this adjustment are located ogether with the fieldstrength adjustment in one byte. This gives the possibility to perform an optimization step during the production of the carradio where the channel separation in relation to the fieldstrength control are trimmed.

The setup of the Stereoblend characteristics, which is programmable in a wide range, is described in 2.8.

De-emphasis and Highcut.

One filter is provided to realize de-emphasis and High-Cut filtering.

The lowpass filter for the de-emphasis allows to choose between a time constant of 50us and 75us.

The filter time constant can further be controlled in both cases over the range $\tau = 2\ \tau_{DEEMPH}$. The control is automatically performed as a function of the filtered field strength level: inside the highcut control range (between VHCH and VHCL) the level is converted into a 5 bit word which drives the lowpass time constant. The FM highcut function can be switched off by I^2C bus (bit 0,of APSD data byte 11). The setup of the highcut characteristics is described in 2.9.

In AM the high-cut filter can be programmed (bit 3 to 7 of APSD data byte 16) to a fixed value (inside the above-mentioned programmable range) in order to provide the desired lowpass characteristic of the AM signal.

PLL and Pilot Tone Detector

The PLL is tasked with locking on the 19kHz pilot tone during a stereo transmission to allow the correct demodulation. The detector enables the stereo demodulation if the pilot tone reaches the selected pilot tone threshold V_{PTHST}. Two different thresholds are available. The detector output can be checked by reading the status byte of the TDA7407 via I^2C bus.

Fieldstrength Control

The filtered field strength signal is fed to the stereo decoder where it can be finely adjusted and normalized so that it can be used to control the highcut and stereoblend functions. Furthermore the adjusted signal can also be used to control the noise-blanker thresholds. The unfiltered field strength meter, on the other hand, is used as input for the stereo decoder multipath detector. These additional functions are described in sections 3.3 and 4.

LEVEL Input and Gain

To help suppress undesired high frequency modulation of the highcut and stereoblend functions the tuner filtered field strength signal (LEVEL) is lowpassed by a combination of a 1st order RC low-pass at 53kHz (working as anti-aliasing filter) and a 1st-order switched capacitor lowpass at 2.2kHz.

The second stage is a programmable gain stage to finely adapt the LEVEL signal internally against tuner spread (see Testmode section 5 LEVELINTERN). The gain is widely programmable in 16 steps from 0dB to 10dB (step = 0.67dB).

Stereoblend Control

The stereoblend control block converts the internal LEVEL voltage (LEVELINTERN) into a demodulator-compatible analog signal which is used to control the channel separation between 0dB and the maximum separation. This control range has a fixed upper limit which is the internal reference voltage REF5V. The lower limit can be programmed between 29.2% and 58% of REF5V in 4.167% steps (see figs. 14, 15).

To adjust the LEVEL voltage to the proper range two values must be defined: the LEVEL gain L_G and VSBL (see fig. 15). To adjust the voltage where the full channel separation is reached (VST) the LEVEL gain L_G has to be defined. The following equation can be used to estimate the gain:

$$LG = \frac{REF5V}{Fieldstrengthvoltage[STEREO]}$$

The gain L_G can be programmed with 4 bits. The MONO voltage VMO (0dB channel separation) can be chosen selecting VSBL. All the necessary internal reference voltages like REF5V are derived from a bandgap circuit, therefore they have a temperature coefficient which is practically zero.

Highcut Control

The highcut control setup is similar to the stereoblend control setup : the starting point VHCH can be set with 2 bits to be 42, 50, 58 or 66% of REF5V whereas the range can be set to be 17, 22, 28 or 33% of VHCH (see fig. 19).

4.6 NOISE-BLANKER

In the automotive environment the MPX signal is disturbed by spikes produced for example by the ignition and by the wiper motor. The aim of the noiseblanker part is to cancel the audible influence of these spikes. To perform this function the output of the stereodecoder is held at the curent voltage for a time between 22 and 38us (programmable). The block diagram of the noiseblanker is shown in fig.20. In the first stage the spikes are detected but to avoid a wrong triggering on high frequency (white) noise a complex trigger desensitization control is implemented. Behind the trigger stage a pulse former generates the "blanking" pulse

Trigger Path

The incoming MPX signal is highpassed by a filter with a corner frequency of 140kHz, amplified and rectified. The rectified signal (RECT) is lowpassed to generate the signal PEAK. Also noise at a frequency higher than 140kHz increases PEAK. The lowpass output voltage can be adjusted by changing the noise rectifier discharge current. The PEAK voltage is fed to a threshold generator which adds to the PEAK voltage a constant voltage VTH, thus producing the trigger threshold PEAK+VTH. Both RECT and PEAK+VTH are fed to a comparator which trig-gers a re-triggerable monoflop. The monoflop output activates the sample-and-hold circuits in the signalpath for a selectable duration.

Automatic Noise Controlled Threshold Adjustment (ATC)

There are mainly two independent possibilities to program the trigger threshold:

a) programming the so-called “low threshold” in 8 steps;
b) programming the so-called “noise-adjusted threshold” in 4 steps

The “low threshold” is active in combination with a good MPX signal without any noise; the PEAK voltage is less than 1V. The sensitivity in this operating mode is high.

If the MPX signal is noisy the PEAK voltage increases due to the higher noise, which is also rectified. With increasing of the PEAK voltage the trigger threshold increases, too. This particular mechanism (“noise-adjusted threshold”) is programmable in 4 steps.

AUTOMATIC THRESHOLD CONTROL MECHANISM

Automatic Threshold Control by the Stereoblend Voltage

Besides the noise-controlled threshold adjustment there is an additional possibility to influence the trigger threshold which depends on the stereoblend control.

The point where the MPX signal starts to become noisy is fixed by the RF part. Therefore also the starting point of the normal noise-controlled trigger adjustment is fixed. In some cases the behavior of the noiseblanker can be improved by increasing the threshold even in a region of higher fieldstrength. Sometimes a wrong triggering occures for the MPX signal often shows distortion in this range which can be avoided even if using a low threshold. Because of the overlap of this range and the range of the stereo/mono transition it can be controlled by stereoblend. This threshold increase is programmable in 3 steps or switched off.

Over Deviation Detector

If the system is tuned to stations with a high deviation the noiseblanker might be erroneously triggered on the higher frequencies of the modulation. To avoid this unnecessary muting of the signal, the noiseblanker offers a deviation-dependent threshold adjustment.

By rectifying the MPX signal a further signal representing the actual deviation is obtained. This is used to increase the PEAK voltage. The circuit offset, gain (and enabling) are programmable in 3 steps.

4.7 MULTIPATH DETECTOR

Using the stereo decoder multipath detector the audible effects of a multipath condition can be minimized. A multipath condition is detected by rectifying the 19kHz spectrum in the fieldstrength signal. An external capacitor is used to define the attack and decay times (see block diagram fig. 21). The pin #MULTIPATHTC is externally connected to a capacitor of about 47nF and the MPIN signal is internally connected to the unfiltered field strength.

To avoid losing the information stored in the external capacitor during AF checks but at the same time to allow some fast multipath detection capability during the same AF check period, the external capacitor is disconnected by the MP-Hold switch. This switch is controlled directly by the pin #RDSMUTE.

Moreover, selecting the "internal influence" in the configuration byte, the channel separation is automatically reduced during a multipath condition according to the voltage appearing at the pin #MULTIPATHTC.

Programming

To obtain a good multipath performance an adaptation is necessary. Therefore tha gain of the 19kHz bandpass is programmable in four steps as well as the rectifier gain. The attack and decay times can be set by properly choosing the value of the external capacitor.

4.8 QUALITY DETECTOR

The device offers a quality detector output voltage representing the quality of the FM reception conditions. This voltage is derived from MPX noise information and multipath information according to the following formula:

Quality = 1.6 (V_{noise} -0.8V)+ a (REF5V-V_{MPOUT})

The noise signal is the PEAK signal of the noise blanker without additional influences. The multipath information weight "a" can be programmed between 0.7 and 1.15. The circuit output pin #QUALITY is a low impedance output able to drive external circuitry as well as suitable to be simply fed to an A/D converter for RDS applications.

AF Search Control

The device is supplied with several functionality to support AF-checks using the stereodecoder. As already mentioned before the high ohmic mute feature at the stereo decoder input avoids any clicks during the jump condition.

It is possible at the same time to evaluate the noise- and multipath-content of the alternate frequency by using the Quality detector output. During this time the multipath detector is automatically switched to a small time constant. One dedicated pin (#RDSMUTE) is provided in order to separate the audioprocessor-mute and stereodecoder AF-functions.

4.9 I^{2}C-Bus Interface

I^{2}C bus protocol is supported. This protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device that controls the transfer is a master and device being controlled is the slave. Th e master will always initiate data transfer and provide the clock to transmit or receive operations. The present device always acts as slave, both in transmission and in reception mode.

Data Transition

Data transition on the SDA line must only occur when the clock SCL is LOW. SDA transitions while SCL is HIGH will be interpreted as START or STOP condition.

Start Condition

A start condition is defined by a HIGH to LOW transition of the SDA line while SCL is at a stable HIGH level. This "START" condition must precede any command and initiate a data transfer onto the bus. The device continuously monitors the SDA and SCL lines for a valid START and will not response to any command if this condition has not been met.

Stop Condition

A STOP condition is defined by a LOW to HIGH transition of the SDA while the SCL line is at a stable HIGH level. This condition terminates the communication between the devices and forces the bus interface of the device into the initial condition.

Acknowledge

Indicates a successful data transfer. The transmitter will release the bus after sending 8 bits of data. During the 9th clock cycle the receiver will pull the SDA line to LOW level to indicate it received the eight bits of data.

Data Transfer

During data transfer the device samples the SDA line on the leading edge of the SCL clock. Therefore, for proper device operation the SDA line must be stable during the SCL LOW to HIGH transition.

Device Addressing

To start the communication between two devices, the bus master must initiate a start instruction sequence, followed by an eight bit word corresponding to the address of the device. The device recognizes the following two addresses:

1100010d tuner part address
1000110d stereo decoder / audio processor address (APSD)

The last bit of the start instruction defines the type of operation to be performed:

- when set to "1", a read operation is selected (data are transferred from the device to the master)
- when set to "0", a write operation is selected (data are transferred from the mas ter to the device)

The device connected to the bus will compare its own hardwired addresses with the slave address being transmitted after detecting a START condition. After this comparison, the device will generate an "acknowledge" on the SDA line and will perform either a read or a write operation according to the state of the R/W bit.

Write Operation
Following a START condition the master sends a slave address word with the R/W bit set to "0". The device will generate an "acknowledge" after this first transmission and will wait for a second word (the subaddress field). This 8-bit address field provides an access to any of the 64 internal addresses (32 corresponding to the tuner address and 32 corresponding to the stereo decoder / audio processor address). Upon receipt of the subaddress the device will respond with an "acknowledge". At this time, all the following words transmitted to the device will be considered as Data. The internal address may be automatically incremented if the auto-increment mode is selected (bit S5 of the subaddress word) . After each word has been received the device will answer with an "acknowledge".

Read Operation
IF the master sends a slave address word with the R/W bit set to "1", the device will transmit one 8-bit data word. This data word content changes according to the address corresponding to the tuner or to the stereo decoder / audio processor. The information are the following:

- tuner
bit0: ISS filter, 1 = ON, 0 = OFF
bit1: ISS filter bandwidth, 1 = 80kHz, 0 = 120kHz
bit2: MPOUT,1 = multipath present, 0 = no multipath
bit3: 1 = PLL is locked in , 0 = PLL is locked out
bit4: fieldstrength indicator, 1 = lower as softmute threshold, 0 = higher as softmute threshold
bit5: adjacent channel indicator, 1 = adjacent channel present, 0 = no adjacent channel
bit6: deviation indicator, 1 = strong overdeviation present, 0 = no strong overdeviation
bit7: deviation indicator, 1 = overdeviation present, 0 = no overdeviation

- stereo decoder / audio processor
bit2: Soft Mute status, 1 = ON, 0 = OFF
bit3: Stereo mode, 1 = stereo, 0 = mono

Table 1. ISS Modes

sm	ac	ac+	dev	dev+	ISSon	80KHz
0	0	0	0	0	0	0
0	1	x	0	0	1	1
0	1	x	1	x	1	0
1	x	x	0	0	1	1
1	0	0	1	x	0	0
1	1	x	1	x	1	0

MODE 1

sm	ac	ac+	dev	dev+	ISSon	80KHz
0	0	0	0	0	0	0
0	1	0	0	0	1	0
0	1	1	x	x	1	1
0	1	0	1	x	1	0
1	x	x	0	0	1	1
1	0	0	1	x	0	0
1	1	0	1	x	1	0
1	1	1	1	x	1	1

MODE 2

Figure 5. Softmute Timing

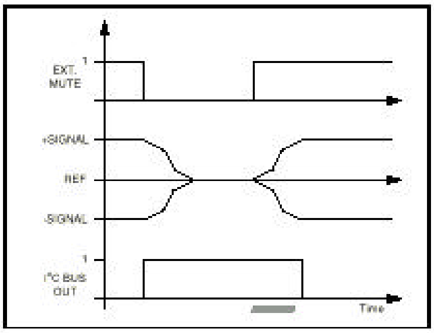


Figure 6. Bass Control @ fc = 80Hz, Q = 1

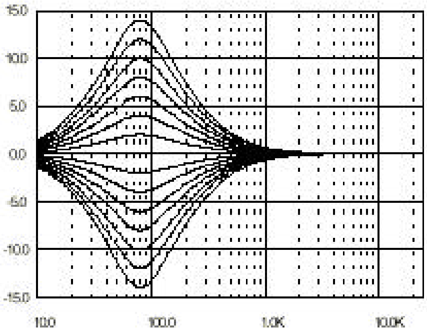


Figure 7. Bass Center @ Gain = 14dB, Q = 1

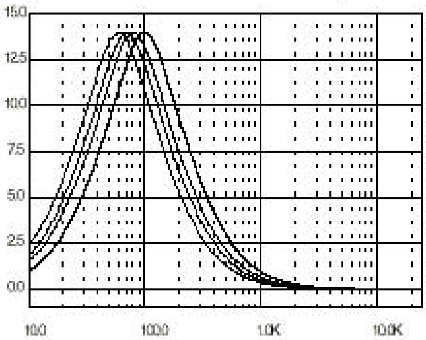


Figure 8. Bass Quality factors @ Gain = 14dB, fc = 80Hz

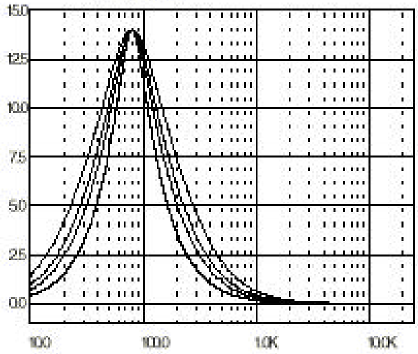
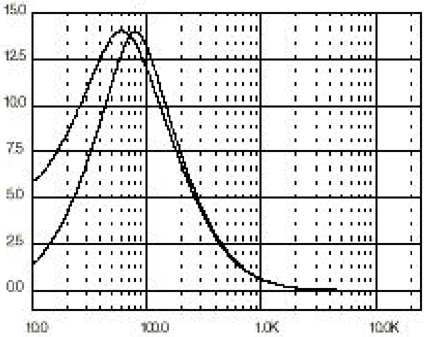


Figure 9. Bass normal and DC Mode @ Gain = 14dB, fc = 80Hz



Note: In general the center frequency, Q and DC-mode can be set independently. The exception from this rule is the mode (5/xx11111xx) where the center frequency is set to 150Hz instead of 100Hz.

Figure 10. Mid Control @ fc=1kHz, Q=1

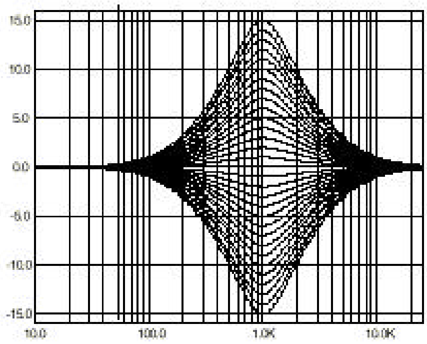


Figure 11. Mid Center Frequency @ Gain=14dB, Q1

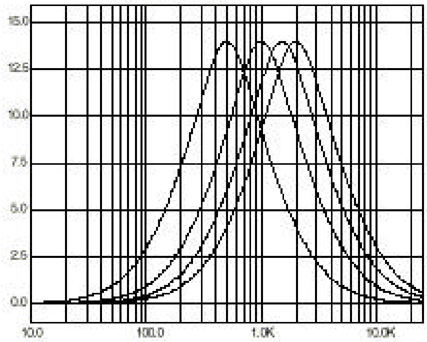


Figure 12. Mid Q-factor @ fc=1kHz, Gain=14dB

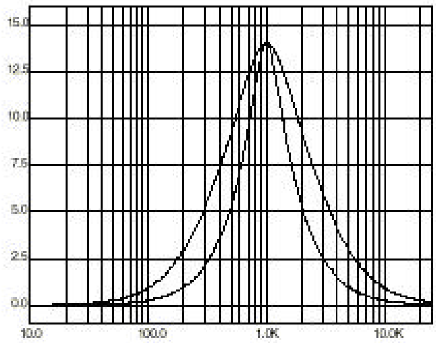


Figure 13. Treble Control @ fc = 17.5KHz

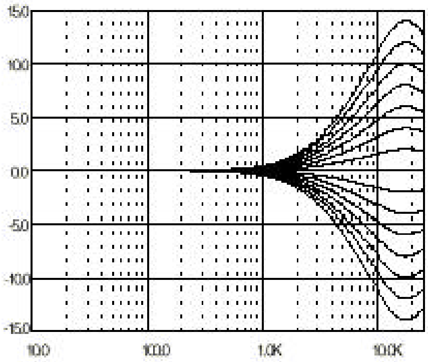


Figure 14. Treble Center Frequencies @ Gain = 14dB

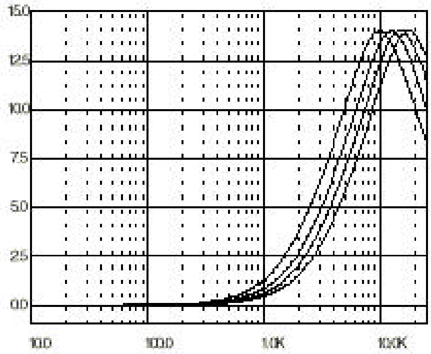


Figure 15. Block Diagram of the Stereodecoder

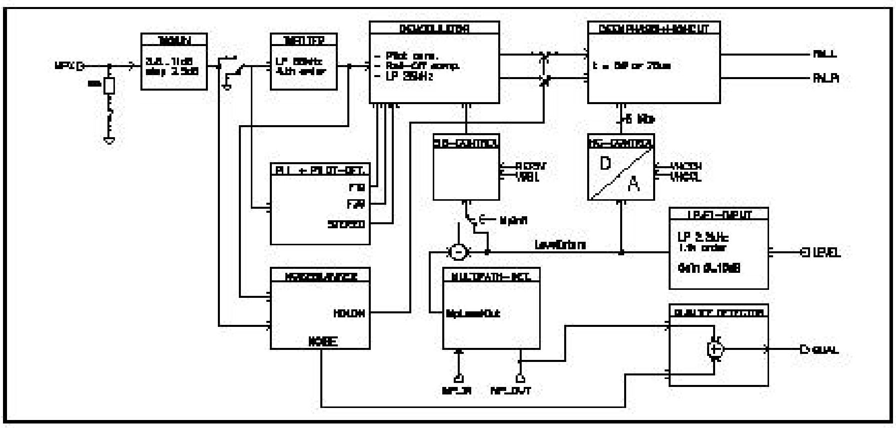


Figure 16. Signals During Stereodecoder's Softmute

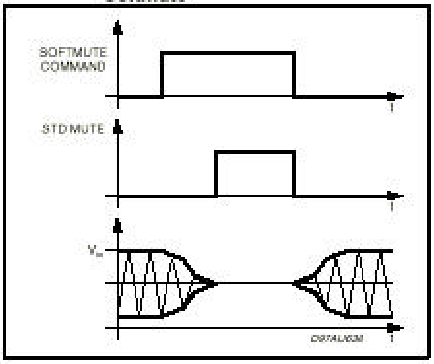


Figure 17. Internal Stereoblend Characteristics

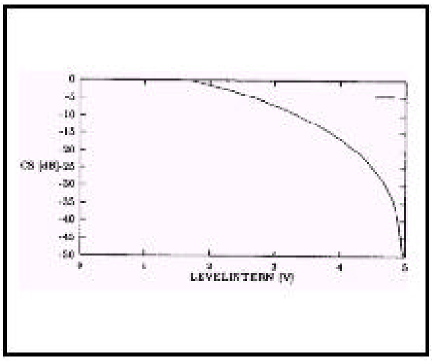


Figure 18. Relationship between unadjusted (LEVEL) and adjusted (LEVELITERN) filtered field strength signals

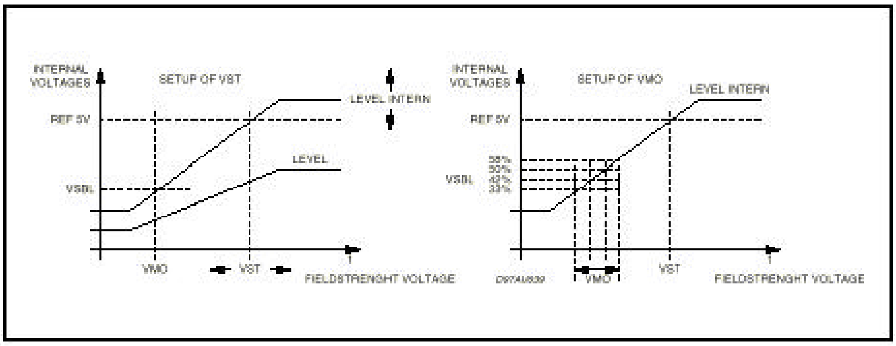


Figure 19. Highcut Characteristics

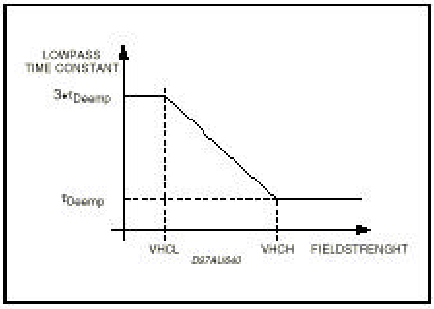


Figure 20. Block Diagram of the Noiseblanker

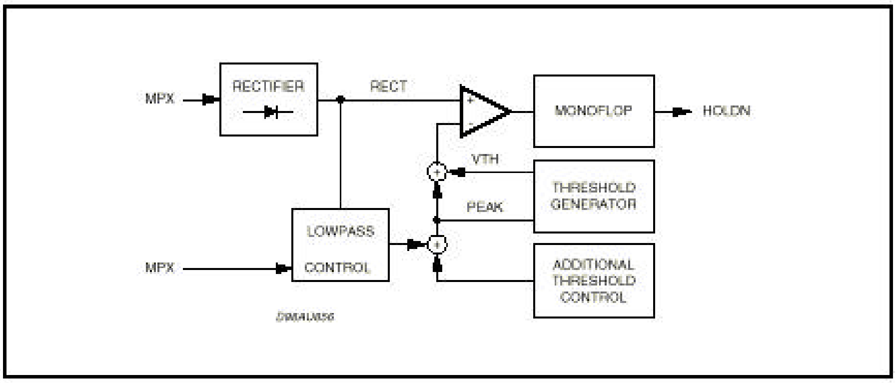
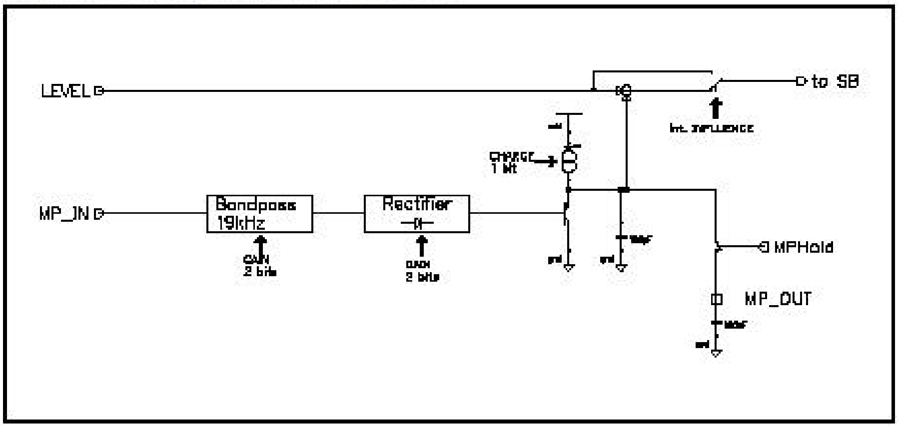


Figure 21. Block Diagram of the Multipath Detector



5.0 SOFTWARE SPECIFICATIONS

5.1 ADDRESS ORGANIZATION (TUNER SECTION)

<table>
<tr><th></th><th>MSB</th><th></th><th></th><th></th><th></th><th></th><th></th><th>LSB</th><th>FUNCTION</th></tr>
<tr><th>SUBADDRESS</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th></th></tr>
<tr><td>0</td><td>STBY</td><td>Current select</td><td colspan="2">Low current</td><td colspan="4">High current</td><td>Charge Pump Control and STBY</td></tr>
<tr><td>1</td><td>Lock det enable</td><td colspan="2">activation delay</td><td colspan="2">phase difference threshold</td><td>AM/FM</td><td>fref BYPASS</td><td>VCOadj clockenab</td><td>PLL Lock Detector,FM mode and tests</td></tr>
<tr><td>2</td><td colspan="8">counter LSB</td><td>PLL Counter 1 (LSB)</td></tr>
<tr><td>3</td><td colspan="8">counter MSB</td><td>PLL Counter 2 (MSB)</td></tr>
<tr><td>4</td><td colspan="8">counter LSB</td><td>PLL Reference Counter 1 (LSB)</td></tr>
<tr><td>5</td><td colspan="8">counter MSB</td><td>PLL Reference Counter 2 (MSB)</td></tr>
<tr><td>6</td><td>FM ISS DD disable thr @ weak FS</td><td colspan="2">FM audio amp mute depth</td><td colspan="5">FM antenna adjustment</td><td>FM Antenna Adjustment and FM Mute Depth</td></tr>
<tr><td>7</td><td>SEEK</td><td colspan="2">AM prescaler</td><td colspan="5">FM RF adjustment</td><td>FM RF Adjustment, AM prescaler and Seek</td></tr>
<tr><td>8</td><td colspan="4">AM stop station</td><td>IFC enable</td><td colspan="3">Δf</td><td>IF Counter Control 1 and AM S.S. Threshold</td></tr>
<tr><td>9</td><td colspan="3">t SAMPLE</td><td colspan="5">f CENTER</td><td>IF Counter Control 2 (central frequency and sampling time)</td></tr>
<tr><td>10</td><td colspan="8">counter LSB</td><td>IF Counter Reference (LSB)</td></tr>
<tr><td>11</td><td colspan="2">IFC AM / FM</td><td colspan="6">counter MSB</td><td>IF Counter Reference (MSB) and IF Counter Mode Select</td></tr>
<tr><td rowspan="2">12</td><td colspan="5" rowspan="2">AM UNAGC</td><td colspan="3">AMIF2amp</td><td rowspan="2">AM Ultra Narrow AGC Threshold, AM IF2 Amplifier Gain, FM SoftMute Enable and AC test</td></tr>
<tr><td></td><td>test ACmute</td><td>FM SMut enable</td></tr>
<tr><td rowspan="2">13</td><td rowspan="2">MPQUAL test</td><td colspan="2">FM demod noise blanker</td><td colspan="5" rowspan="2">FM demodulator fine adjust</td><td rowspan="2">FM Demodulator Adjust, FM demod noise blanker and MPtest</td></tr>
<tr><td>AM Smeter extens</td><td></td></tr>
<tr><td>14</td><td colspan="2">ISS AC narrowband threshold</td><td colspan="3">ISS AC wideband threshold</td><td>ISS AC gain</td><td>ISS AC HP/BP</td><td>ISS 30KHz on</td><td>Quality Detection Adjacent Channel</td></tr>
<tr><td>15</td><td>ISS MP defeat AC</td><td colspan="2">ISS mode</td><td colspan="2">ISS MP threshold</td><td>test Smet unfiltered</td><td>ISS MP center</td><td>ISS MP ctrl on</td><td>Quality Detection Multipath</td></tr>
<tr><td>16</td><td>*0*</td><td colspan="2">ISS DD off threshold</td><td colspan="2">ISS DD narrow/wide threshold</td><td colspan="3">ISS DD time constant</td><td>Quality Detection Deviation</td></tr>
<tr><td>17</td><td colspan="2">ISS center</td><td colspan="3">ISS time constant</td><td>ISS 80/120</td><td>ISS on</td><td>ISS enable</td><td>Quality ISS Filter</td></tr>
<tr><td>18</td><td colspan="2">SD mode</td><td colspan="2">ISS MP gain</td><td>VCO adj start</td><td colspan="3">test PLL</td><td>PLL test, 456KHz VCO adjustment start (auto mode)</td></tr>
<tr><td>19</td><td>manual/ auto</td><td colspan="5">manual VCO frequency</td><td>man SET456</td><td>man ENIFC</td><td>456KHz VCO adjustment (manual mode)</td></tr>
<tr><td>20</td><td colspan="4">FM stop station</td><td colspan="4">FM soft mute</td><td>FM Stop Station and Soft Mute Thresholds</td></tr>
<tr><td>21</td><td>AC QUAL test</td><td colspan="4">AdjChan mute clamp</td><td colspan="3">AdjChan mute gain</td><td>Adjacent mute gain, clamping threshold and test</td></tr>
<tr><td>22</td><td colspan="3">AM Smeter filter TC</td><td colspan="5">FMSmslider</td><td>FM Smeter slider and AM Smeter filter Time Constant</td></tr>
<tr><td>23</td><td colspan="4">IFT2 adjust</td><td colspan="4">IFT1 adjust</td><td>IFT adjust</td></tr>
<tr><td>24</td><td colspan="2">FMIFamp2</td><td>Clksep</td><td colspan="5">XTAL adjustment</td><td>XTAL adjustment and FM IF Amp2</td></tr>
</table>

25	AM WAGC		FMNAGCkey	AM WAGC and FM NAGC keying
26	AM NAGC		FM demod ref frequency divider	AM NAGC and FM demod ref frequency divider
27	test ISS			ISS testing
28	ISS filter test	test ISS MP/AC	test ISS	ISS testing
29	Smeter pins test	test TUNER		Tuner and Smeter tests
30	AdjChan mute disable @ low FS	AdjChan mute BP/HP	AdjChan mute threshold	Adjacent mute disable, filtering and threshold
31	Tuner quality AdjChan gain	Tuner quality Multipath gain	FS ISS activation	Tuner Quality AdjChannel and Multipath gain, FS ISS Activation

ADDRESS							
MSB							**LSB**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
1	1	0	0	0	1	0	R/W

SUBADDRESS							
MSB							**LSB**
S7	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**
x	x	autoincr	subaddress				

READ MODE: ISS OUTPUTS							
MSB							**LSB**
S7	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**
DEV+	DEV	AC	FS	INLOCK	MP	BW	ON

5.2 SUBADDRESS ORGANIZATION (TUNER SECTION)

SUBADDRESS 0: Charge Pump Control								
MSB							**LSB**	**FUNCTION**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
								CHARGE PUMP
				0	0	0	0	High current = 0mA
				0	0	0	1	High current = 0.5mA
				0	0	1	0	High current = 1mA
				0	0	1	1	High current = 1.5mA
				-	-	-	-	-
				1	1	1	1	High current = 7.5mA
		0	0					Low current = 0uA
		0	1					Low current = 50uA
		1	0					Low current = 100uA
		1	1					Low current = 150uA
	0							Select low current
	1							Select high current
								TUNER STAND-BY
0								Tuner StandBy OFF
1								Tuner StandBy ON

SUBADDRESS 1: PLL Lock Detector, FM mode and test								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
							0	VCO adjust Clock Disable
							1	VCO adjust Clock Enable
						0		fref BYPASS disable
						1		fref BYPASS enable
								TUNER/PLL AM/FM MODE
					0			Select AM mode
					1			Select FM mode
								LOCK DETECTOR CONTROL
			0	0				PD phase difference threshold 10ns
			0	1				20ns
			1	0				30ns
			1	1				40ns
	0	0						Not valid
	0	1						Activation delay 4 x $1/f_{REF}$
	1	0						6 x $1/f_{REF}$
	1	1						8 x $1/f_{REF}$
0								Lock detector doesn't control charge pump
1								Lock detector controls charge pump

SUBADDRESS 2: PLL Counter 1 (LSB)								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	LSB = 0
0	0	0	0	0	0	0	1	LSB = 1
0	0	0	0	0	0	1	0	LSB = 2
-	-	-	-	-	-	-	-	-
1	1	1	1	1	1	0	0	LSB = 252
1	1	1	1	1	1	0	1	LSB = 253
1	1	1	1	1	1	1	0	LSB = 254
1	1	1	1	1	1	1	1	LSB = 255

SUBADDRESS 3: PLL Counter 2 (MSB)								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	MSB = 0
0	0	0	0	0	0	0	1	MSB = 256
0	0	0	0	0	0	1	0	MSB = 512
-	-	-	-	-	-	-	-	-
1	1	1	1	1	1	0	0	MSB = 64768
1	1	1	1	1	1	0	1	MSB = 65024
1	1	1	1	1	1	1	0	MSB = 65280
1	1	1	1	1	1	1	1	MSB = 65536
Note: 1. Swallow mode: f_{VCO}/f_{SYN} = LSB + MSB + 32								

SUBADDRESS 4: PLL Reference Counter 1 (LSB)								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	LSB = 0
0	0	0	0	0	0	0	1	LSB = 1
0	0	0	0	0	0	1	0	LSB = 2
-	-	-	-	-	-	-	-	-
1	1	1	1	1	1	0	0	LSB = 252
1	1	1	1	1	1	0	1	LSB = 253
1	1	1	1	1	1	1	0	LSB = 254
1	1	1	1	1	1	1	1	LSB = 255

SUBADDRESS 5: PLL Reference Counter 2 (MSB)								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	MSB = 0
0	0	0	0	0	0	0	1	MSB = 256
0	0	0	0	0	0	1	0	MSB = 512
-	-	-	-	-	-	-	-	-
1	1	1	1	1	1	0	0	MSB = 64768
1	1	1	1	1	1	0	1	MSB = 65024
1	1	1	1	1	1	1	0	MSB = 65280
1	1	1	1	1	1	1	1	MSB = 65536
Note: 1. f_{OSC}/f_{REF} = LSB + MSB + 1								

SUBADDRESS 6: FM Antenna Adjustment and FM Mute Depth								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								FM antenna adj (proportional to Vtuning)
			0	1	1	1	1	-30%
			0	1	1	1	0	-28%
			-	-	-	-	-	-
			0	0	0	0	1	-2%
			0	0	0	0	0	-0%
			1	0	0	0	0	+0%
			1	0	0	0	1	+2%
			-	-	-	-	-	-
			1	1	1	1	0	+28%
			1	1	1	1	1	+30%
								FM Soft Mute Depth
	0	0						25 dB
	1	0						20 dB
	0	1						16 dB
	1	1						13.5 dB
								ISS deviation detector disabling threshold relative to weak field ISS activation threshold (byte 31 bit 3-0)
0								-100 mV
1								+100 mV

SUBADDRESS 7: FM RF Adjustment, AM Prescaler and Seek								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								FM RF adj (proportional to Vtuning)
			0	1	1	1	1	-30%
			0	1	1	1	0	-28%
			-	-	-	-	-	-
			0	0	0	0	1	-2%
			0	0	0	0	0	-0%
			1	0	0	0	0	+0%
			1	0	0	0	1	+2%
			-	-	-	-	-	-
			1	1	1	1	0	+28%
			1	1	1	1	1	+30%
								AM VCO divider ratio
	0	0						10
	0	1						8
	1	0						6
	1	1						4
								SEEK MODE
0								Seek OFF
1								Seek ON

SUBADDRESS 8: IF Counter Control 1 and AM S.S. Threshold

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								IF COUNTER CONTROL
					0	0	0	Not valid
					0	0	1	Not valid
					0	1	0	Not valid
					0	1	1	Δf = 6.25kHz (FM) 1kHz (AM UPC)
					1	0	0	Δf = 12.5kHz (FM) 2kHz (AM UPC)
					1	0	1	Δf = 25kHz (FM) 4kHz (AM UPC)
					1	1	0	Δf = 50kHz (FM) 8kHz (AM UPC)
					1	1	1	Δf = 100kHz (FM) 16kHz (AM UPC)
				0				IF counter disable / stand by
				1				IF counter enable
								AM Stop Station Threshold
0	0	0	0					0 mV
0	0	0	1					150 mV
-	-	-	-					- -
1	1	1	0					2100 mV
1	1	1	1					2250 mV

SUBADDRESS 9: IF Counter Control 2

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
			0	0	0	0	0	f_{Center} = 10.60625MHz (FM) 449KHz (AM)
			0	0	0	0	1	f_{Center} = 10.61250MHz (FM) 450KHz(AM)
			-	-	-	-	-	-
			0	1	0	1	0	f_{Center} = 10.66875MHz (FM) 459KHz(AM)
			0	1	0	1	1	f_{Center} = 10.67500MHz (FM) 460KHz (AM)
			0	1	1	0	0	f_{Center} = 10.68125MHz (FM) 461KHz (AM)
			0	1	1	0	1	f_{Center} = 10.68750MHz (FM) 462KHz (AM)
			0	1	1	1	0	f_{Center} = 10.69375MHz (FM) 463KHz (AM)
			0	1	1	1	1	f_{Center} = 10.70000MHz (FM) 464KHz (AM)
			1	0	0	0	0	f_{Center} = 10.70625MHz (FM) 465KHz (AM)
			1	0	0	0	1	f_{Center} = 10.71250MHz (FM) 466KHz (AM)
			-	-	-	-	-	-
			1	1	1	1	1	f_{Center} = 10.80000MHz (FM) 480KHz (AM)
0	0	0						t_{Sample} = 20.48ms (FM) 128ms (AM)
0	0	1						t_{Sample} = 10.24ms (FM) 64ms (AM)
0	1	0						t_{Sample} = 5.12ms (FM) 32ms (AM)
0	1	1						t_{Sample} = 2.56ms (FM) 16ms (AM)
1	0	0						t_{Sample} = 1.28ms (FM) 8ms (AM)
1	0	1						t_{Sample} = 640ms (FM) 4ms (AM)
1	1	0						t_{Sample} = 320ms (FM) 2ms (AM)
1	1	1						t_{Sample} = 160ms (FM) 1ms (AM)

SUBADDRESS 10: IF Counter Reference (LSB)

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	LSB = 0
0	0	0	0	0	0	0	1	LSB = 1
0	0	0	0	0	0	1	0	LSB = 2
-	-	-	-	-	-	-	-	-
1	1	1	1	1	1	0	0	LSB = 252
1	1	1	1	1	1	0	1	LSB = 253
1	1	1	1	1	1	1	0	LSB = 254
1	1	1	1	1	1	1	1	LSB = 255

SUBADDRESS 11: IF Counter Reference (MSB) and IF Counter Mode Select								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
		0	0	0	0	0	0	MSB = 0
		0	0	0	0	0	1	MSB = 256
		0	0	0	0	1	0	MSB = 512
		-	-	-	-	-	-	-
		1	1	1	1	0	1	MSB = 15616
		1	1	1	1	1	0	MSB = 15872
		1	1	1	1	1	1	MSB = 16128
								IF COUNTER MODE
0	0							Not valid
0	1							IF counter FM mode (10.7KHz)
1	0							IF counter AM mode (450KHz)
1	1							Not valid
Note: 1. f_{OSC} / f_{TIM} = LSB + MSB + 1								

SUBADDRESS 12: AM IF Amplifier Gain and Ultra Narrow Band AGC Threshold, FM Smeter and AC test								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								test FM FS soft mute enable (FM mode) [bit shared with AM IF AMP Gain]
							0	FS Soft mute disabled
							1	FS Soft mute enabled
								test AC Mute (FM mode) [bit shared with AM IF AMP Gain]
						0		test mode: FM demod Vout is disconnected from users
						1		no test (std)
								AM IF AMP Gain (AM mode)
					0	0	0	Not used
					0	0	1	53.2 dB
					0	1	0	55.8 dB
					0	1	1	60.2 dB
					1	0	0	58.3 dB
					1	0	1	61.7 dB
					1	1	0	62.8 dB
					1	1	1	64.8 dB
								AM UNAGC enable
				1				Enable AM UNAGC
				0				Disable AM UNAGC
								AM Ultra Narrow Band AGC Threshold
0	0	0	0					74.4 dBuV @SG
0	0	0	1					78.8 dBuV @SG
0	0	1	0					80 dBuV @SG
0	0	1	1					80.7 dBuV @SG 119.5dBuV @ IF2AMPOUT
0	1	0	0					53.2 dBuV @SG
0	1	0	1					77.1 dBuV @SG
0	1	1	0					78.5 dBuV @SG
0	1	1	1					79.4 dBuV @SG
1	0	0	0					42.7 dBuV @SG
1	0	0	1					65.8 dBuV @SG
1	0	1	0					77.6 dBuV @SG
1	0	1	1					78.5 dBuV @SG
1	1	0	0					32.6 dBuV @SG 113.5dBuV @ IF2AMPOUT
1	1	0	1					55 dBuV @SG
1	1	1	0					73.3 dBuV @SG
1	1	1	1					77.6 dBuV @SG

SUBADDRESS 13: Demodulator Fine Adjust and Noise Blanker, MPQual test									
MSB							LSB	FUNCTION	
D7	D6	D5	D4	D3	D2	D1	D0		
								FM audio demodulator current adjust	
			0	0	0	0	0	+0 uA	
			0	0	0	0	1	+0.167 uA	
			-	-	-	-	-	- uA	
			0	1	1	1	1	+2.51 uA	
			1	0	0	0	0	-0 uA	
			1	0	0	0	1	-0.167 uA	
			1	-	-	-	-	- uA	
			1	1	1	1	1	-2.51 uA	
								Demodulator Noise Blanker	**AM Smeter extension**
	0	0						NB1&2 on (impvic&lontmas)	old (10.7 MHz)
	0	1						NB1 on (impvicmas)	old (10.7 MHz)
	1	0						NB2 on (implontmas)	new (450 kHz)
	1	1						NB1&2 off	new (450 kHz)
								Multipath (ISS) test	
0								MP test OFF	
1								MP test ON (ISS qualitydetector MP input from #ACinL, ISS MP filter+rect output to Smeter test muxer if input 12 is selected)	

SUBADDRESS 14: Quality Detection Adjacent Channel									
MSB							**LSB**	**FUNCTION**	
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
								ISS filter for WB	
							0	ISS filter 30KHz OFF	
							1	ISS filter 30KHz ON	
								ISS Adjacent Channel filter configuration	
						0		AC highpass frequency 100KHz	
						1		AC bandpass frequency 100KHz	
					0			AC gain	32 dB
					1				38 dB
								ISS Adjacent Channel thresholds	
		0	0	0				AC **wide band** threshold	0.25 V
		0	0	1					0.35 V
		0	1	0					0.45 V
		-	-	-				-	-
		1	1	1					0.95 V
0	0							AC **narrow band** threshold	0 V
0	1								0.1 V
1	0								0.2 V
1	1								0.3 V

SUBADDRESS 15: Quality Detection Multipath and Smeter test									
MSB							**LSB**	**FUNCTION**	
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
								ISS Multipath control enabling	
							0	Multipath control	ON
							1		OFF
								ISS Multipath filter center frequency	
						0		MP Bandpass frequency	19 KHz
						1			31 KHz
								ISS Multipath filter input selector (test mode)	
					0			Smeter unfilt test OFF	
					1			Smeter unfilt test ON	
								ISS Multipath threshold	
			0	0					0.5 V
			0	1					0.75 V
			1	0					1 V
			1	1					1.25 V
								ISS mode	
	0	0						Application mode1	
	0	1						Application mode2	
								ISS Multipath control mode	
0								MP control AC+ detection	
1								MP control the AC and AC+ detection	

SUBADDRESS 16: Quality Detection Deviation										
MSB							**LSB**	**FUNCTION**		
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**			
								ISS deviation detector time constant		
					0	0	0	charge current;discharge current	34uA	6uA
					0	0	1		32uA	8uA
					0	1	0		30uA	10uA
					1	0	0		26uA	14uA
					1	1	1		20uA	20uA
								ISS deviation detector thresholds		
			0	0				DEV Threshold for ISS **narrow-wide**	30 KHz	
			0	1					45 KHz	
			1	0					60 KHz	
			1	1					75 KHz	
	0	0						DEV Threshold for ISS filter **OFF** ratio	1	
	0	1							1.3	
	1	0							1.4	
	1	1							1.5	
0								not used		
1								AUX set int80		

SUBADDRESS 17: Quality ISS Filter								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								ISS automatic control from AC detector
							0	ON (AC drives ISSTC
							1	OFF (AC has no inlfuence on ISSTC)
								ISS manual control
						0		automatic control only
						1		manual force filter ON
					0			manual force BW 120 KHz
					1			manual force BW 80 KHz
								ISS time constant
								current: discharge chrg mid chrg narrw
		0	0	0				1uA 74uA 124uA
		0	0	1				3uA 72uA 122uA
		0	1	0				5uA 70uA 120uA
		1	0	0				9uA 66uA 116uA
		1	1	1				15uA 60uA 110uA
								ISS filter center frequency
0	0							shift from 450 kHz -20 KHz
0	1							-10 KHz
1	0							0 KHz
1	1							+10 KHz

SUBADDRESS 18: PLL test, 456KHz VCO adjust start, ISS MP Gain and SD out mode								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								PLL TEST MODE
					0	0	0	
					0	0	1	
					0	1	0	
					0	1	1	
					1	0	0	
					1	0	1	
					1	1	0	
					1	1	1	
								Automatic 456 kHz VCO adjustment
				0				Waiting
				1				START
								ISS Multipath filter gain
		0	0					ISS MP Gain 2 dB
		0	1					13 dB
		1	0					16 dB
		1	1					19 dB
								SD pin configuration
0	0							SS (IFC and FM SM Stop)
0	1							IFCounter out
1	0							FM Smeter Stop
1	1							Logic 1

SUBADDRESS 19: 456KHz VCO adjustment (manual mode)									
MSB							LSB	FUNCTION	
D7	D6	D5	D4	D3	D2	D1	D0		
							0	Enable IFC (I2CBUS)	OFF
							1		ON
						0		Enable 456KHz VCO adj procedure (I2CBUS)	OFF
						1			ON
	0	0	0	0	0			VCO 456KHz frequency adjust (I2CBUS)	minfreq
	0	0	0	0	1				
	-	-	-	-	-				
	0	1	1	1	1				
	1	0	0	0	0				
	-	-	-	-	-				
	1	1	1	1	0				
	1	1	1	1	1				maxfreq
0								Manual adjustment procedure (I2CBUS)	
1								Automatic adjustment procedure (State Machine)	

SUBADDRESS 20: FM Stop Station and Soft Mute Thresholds								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								Soft Mute Threshold on Smeter
				0	0	0	0	0 mV
				0	0	0	1	100 mV
				-	-	-	-	- -
				1	1	1	0	1.4 V
				1	1	1	1	1.5 V
								FM Stop Station Threshold on Smeter
0	0	0	0					400 mV
0	0	0	1					800 mV
-	-	-	-					- -
1	1	1	0					3.2 V
1	1	1	1					3.6 V

SUBADDRESS 21: Adjacent Channel Mute								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
					0	0	0	Adj Channel Mute Gain 10.4 dB
					0	0	1	11.4 dB
					0	1	0	12.4 dB
					0	1	1	13.4 dB
					1	0	0	14.4 dB
					1	0	1	15.4 dB
					1	1	0	16.4 dB
					1	1	1	17.4 dB
	0	0	0	0				Adj Channel Mute Clamp 500 mV
	0	0	0	1				600 mV
	-	-	-	-				- -
	1	0	0	0				1.3 V
	-	-	-	-				- -
	1	1	1	0				1.9 V
	1	1	1	1				2 V
								Adjacent Channel (ISS) test
0								AC test OFF
1								AC test ON (ISS qualitydetector AC input from #ACinL, ISS AC filter+rect output to Smeter test muxer if input 12 is selected)

SUBADDRESS 22: FM Smeter Slider and AM Smeter Time Constant								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								FM Smeter Slider
			0	0	0	0	0	0 V
			0	0	0	0	1	0.48 V
			-	-	-	-	-	- -
			1	1	1	1	0	1.45 V
			1	1	1	1	1	1.5 V
								AM Smeter Filter TC (resistor value)
0	0	0						75 KOhm
1	0	0						50 KOhm
0	1	0						35 KOhm
1	1	0						24 KOhm
0	0	1						16 KOhm

SUBADDRESS 23: IFT Adjust								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								IFT1 Adjust
				0	0	0	0	0 pF
				0	0	0	1	0.55 pF
				-	-	-	-	- -
				0	1	1	1	7.7 pF
				1	1	1	1	8.25 pF
								IFT2 Adjust
0	0	0	0					0 pF
1	0	0	0					1.6 pF
-	-	-	-					- -
0	1	1	1					22.4 pF
1	1	1	1					24 pF

SUBADDRESS 24: XTAL and FM IF AMP 2 Gain								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								XTAL adjust Cload
			0	0	0	0	0	0 pF
			0	0	0	0	1	0.625 pF
			0	0	0	1	0	1.25 pF
			0	0	1	0	0	2.5 pF
			0	1	0	0	0	5 pF
			1	0	0	0	0	10 pF
			1	1	1	1	1	10.4 pF
								XTAL TEST
		0						xtal clock
		1						clocksep (testing)
								FM IF Amp2 gain
0	0							6 dB
0	1							8 dB
1	0							10 dB
1	1							not used

SUBADDRESS 25: FM NAGC key and AM WAGC								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								FM Narrow AGC key IF input
					0	0	0	36 dB
					0	0	1	42 dB
					0	1	0	48 dB
					0	1	1	54 dB
					1	0	0	60 dB
					1	0	1	66 dB
					1	1	0	72 dB
					1	1	1	keying OFF
								AM WAGC starting point @ MIX1IN
0	0	0	0	0				88 dBuV
-	-	-	-	-				- -
1	1	1	1	1				106 dBuV

SUBADDRESS 26: AM NAGC key and FM demod ref frequency test								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
					1	1	0	test for FM demod ref freq divider (standard configuration)
								AM NAGC starting point @ MIX2IN
0	0	0	0	0				85 dBuV
-	-	-	-	-				- -
1	1	1	1	1				103 dBuV

SUBADDRESS 27: ISS tests								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								ISS test multiplexer (1)
0	0	0	0	0	0	0	0	no test
0	0	0	0	0	0	0	1	test MPthresholds
0	0	0	0	0	0	1	0	test ACNthresholds
0	0	0	0	0	1	0	0	test DWthresholds
0	0	0	0	1	0	0	0	test Dthresholds
0	0	0	1	0	0	0	0	test ACWthreshold
0	0	1	0	0	0	0	0	test ac
0	1	0	0	0	0	0	0	test MDSCO
1	0	0	0	0	0	0	0	test ISSout

SUBADDRESS 28: ISS test								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								ISS test multiplexer (2)
		0	0	0	0	0	0	no test
		0	0	0	0	0	1	test dev+
		0	0	0	0	1	0	test dev+
		0	0	0	1	0	0	tset refdev
		0	0	1	0	0	0	test demVout
		0	1	0	0	0	0	test ISSin
		1	0	0	0	0	0	test ISSClkEnable
								ISS test in
	0							test in ISS disable
	1							test in ISS enable
								ISS test clock
0								test ISS clock disable
1								test ISS clock enable

SUBADDRESS 29: Tuner and Smeter tests								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								SMETER test multiplexer
		0	0	0	0	0	0	test off
		0	0	0	0	0	1	Test AMAGC1W
		0	0	0	0	1	0	Test AMAGC1N
		0	0	0	0	1	1	Test AMAGC1UN
		0	0	0	1	0	0	Test FMSmuteThreshold
		0	0	0	1	0	1	Test FMSMStop
		0	0	0	1	1	0	Test AMIF2Amp
		0	0	0	1	1	1	Test AMSDDAC
		0	0	1	0	0	0	Test FMKAGC
		0	0	1	0	0	1	Test FMACMDisable
		0	0	1	0	1	0	Test FMDemodAdjON
		0	0	1	0	1	1	Test FMDemodAdjONMute
		0	0	1	1	0	0	Test FMACMuteRct
		0	0	1	1	0	1	Test FSISSONThreshold
		0	0	1	1	1	0	Test FSISSON
		0	0	1	1	1	1	Test ISSInput
	0							Smeter OUT ACD enable
	1							Test SmeterIN
0								Smeter filter force enable
1								Test TMODE1OUT (byte 27/28)

SUBADDRESS 30: Adjacent channel mute								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								Adjacent channel mute threshold
				0	0	0	0	0 mV
				0	0	0	1	28.7 mV
				-	-	-	-	- -
				1	0	0	0	229.3 mV
				-	-	-	-	- -
				1	1	1	0	401.3 mV
				1	1	1	1	430 mV
								Adjacent channel mute filter configuration
			0					AdjChannel Mute HighPass filter 1
			1					AdjChannel Mute BandPass filter 1
		0						AdjChannel Mute HighPass filter 2
		1						AdjChannel Mute BandPass filter 2
								AdjChannel Mute disable @ low FS
0	0							threshold 1 V
0	1							1.33 V
1	0							1.66 V
1	1							2 V

SUBADDRESS 31: Adjacent channel and Multipath gain, weak field ISS threshold								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								Weak field ISS activation threshold
				0	0	0	0	-450 mV
				0	0	0	1	-385.7 mV
				-	-	-	-	- -
				0	1	1	1	-0 mV
				1	0	0	0	+0 mV
				1	0	0	1	+64.28 mV
				-	-	-	-	- -
				1	1	1	0	+385.7 mV
				1	1	1	1	+450 mV
								Tuner Quality Multipath gain
		0	0					0 (OFF) dB
		0	1					-4 dB
		1	0					0 dB
		1	1					+4 dB
								Tuner Quality Adjacent channel gain
0	0							OFF
0	1							-4 dB
1	0							0 dB
1	1							+4 dB

5.3 ADDRESS ORGANIZATION (STEREODECODER AND AUDIOPROCESSOR SECTION)

SUBADDRESS	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	FUNCTION
0	spkr coupl	in gain				source selector			Source selector, in-gain, Speaker coupling
1	volume steps								Volume
2	*not used*	treble center freq		treble steps					Treble
3	bass DC mode	bass Q factor		bass steps					Bass
4	volume steps								Speaker attenuator Left Front
5	volume steps								Speaker attenuator Right Front
6	volume steps								Speaker attenuator Left Rear
7	volume steps								Speaker attenuator Right Rear
8	NB time		bass center frequency		*not used*	soft mute time		I^2C soft mute off	Soft mute, soft mute time, Bass, Noise blanker time
9	deemph.	pilot thr.	NB peak dis	force mono	auto zero status	std in gain		std mute disable	Stereo decoder mute, st. dec. in-gain, mono, NB PEAK disch.curr., pilot thresh., deemph.
10	overdev. adj.		NB on	noise contr. thresh.		low threshold			Noise Blanker
11	mpath. infl.	VHCL		VHCH		max high cut		high cut on	High cut, multipath influence
12	mpath. infl.	Quality del. coeff.		NB field strength gain		NB field strength threshold		*not used*	Fieldstrength control
13	mpath det. Reflect. Gain		mpath charge	mpath int. infl.	mpath det. gain		noise rect. disch. R		Noise rectifier disch.resistor, Multipath det.bandpass gain, multipath internal influence, reflection gain
14	roll-off compens.	level gain				roll-off compensation			Roll-off compensation, level gain
15	AP test ON	400K ON	test signal selection				test SC OFF	StD test ON	TEST BYTE
16	AM high-cut control corner frequency					quality noise gain		mpathtest	AMHCC, Quality noise gain, test
17	mid Q-factor	mid center frequency		mid steps					Mid
18	*not used*	*not used*	*not used*	*not used*	*not used*	VSBL			Stereo blend

SUBADDRESS

MSB							LSB
S7	S6	S5	S4	S3	S2	S1	S0
testcon	azhold	autoincr	subaddress				

READ MODE

MSB							LSB
S7	S6	S5	S4	S3	S2	S1	S0
				STEREO	SMON		

ADDRESS

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	1	1	0	R/W

5.4 SUBADDRESS ORGANIZATION (STEREODECODER AND AUDIOPROCESSOR SECTION)

SUBADDRESS 0: Source selector, in-gain, Speaker coupling								
MSB							**LSB**	**FUNCTION**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
								Source selector
					0	0	0	Quasi-differential input 1
					0	0	1	Quasi-differential input 2
					0	1	0	not used (mute)
					0	1	1	Tuner input (AM mode)
					1	0	0	Tuner input (FM mode)
					1	0	1	not used (mute)
					1	1	0	not used (mute)
					1	1	1	not used (mute)
								In-Gain
	0	0	0	0				0 dB
	0	0	0	1				1 dB
	.	.	.	.				.
	1	1	1	0				14 dB
	1	1	1	1				15 dB
								Speaker Coupling
0								AC (external)
1								DC (internal)

SUBADDRESS 1, 4, 5, 6, 7: Volume, Spkr atten. LF, RF, LR, RR								
MSB							**LSB**	**FUNCTION**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
								Volume steps
1	0	0	0	1	1	1	1	+15 dB
.	.	.	.	.	.	.	.	.
1	0	0	0	0	0	0	1	+1 dB
0	0	0	0	0	0	0	0	0 dB
0	0	0	0	0	0	0	1	-1 dB
.	.	.	.	.	.	.	.	.
0	0	0	0	1	1	1	1	-15 dB
0	0	0	1	0	0	0	0	-16 dB
.	.	.	.	.	.	.	.	.
0	1	0	0	1	1	1	0	-78 dB
0	1	0	0	1	1	1	1	-79dB
x	1	1	x	x	x	x	x	mute

all other combinations not allowed

SUBADDRESS 2: Treble								
MSB							**LSB**	**FUNCTION**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
								Treble filter steps
			0	0	0	0	0	-15 dB
			0	0	0	0	1	-14 dB
			.	.	.	.	.	.
			0	1	1	1	0	-1 dB
			0	1	1	1	1	0 dB
			1	1	1	1	1	0 dB
			1	1	1	1	0	+1 dB
			.	.	.	.	.	.
			1	0	0	0	1	+14 dB
			1	0	0	0	0	+15 dB
								Treble filter center frequency
	0	0						10.0 kHz
	0	1						12.5 kHz
	1	0						15.0 kHz
	1	1						17.5 kHz

SUBADDRESS 3: Bass								
MSB							**LSB**	**FUNCTION**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
								Bass filter steps
			0	0	0	0	0	-15 dB
			0	0	0	0	1	-14 dB
			.	.	.	.	.	.
			0	1	1	1	0	-1 dB
			0	1	1	1	1	0 dB
			1	1	1	1	1	0 dB
			1	1	1	1	0	+1 dB
			.	.	.	.	.	.
			1	0	0	0	1	+14 dB
.	.	.	1	0	0	0	0	+15 dB
								Bass filter Q-factor
	0	0						1.00
	0	1						1.25
	1	0						1.50
	1	1						2 (makes cent. freq. = 150Hz when programmed to 100Hz)
								Bass filter DC mode
0								off
1								on

SUBADDRESS 4: Speaker attenuator Left Front								
MSB							**LSB**	**FUNCTION**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
								Volume steps
1	0	0	0	1	1	1	1	+15 dB
.	.	.	.	.	.	.	.	.
1	0	0	0	0	0	0	1	+1 dB
0	0	0	0	0	0	0	0	0 dB
0	0	0	0	0	0	0	1	-1 dB
.	.	.	.	.	.	.	.	.
0	0	0	0	1	1	1	1	-15 dB
0	0	0	1	0	0	0	0	-16 dB
.	.	.	.	.	.	.	.	.
0	1	0	0	1	1	1	0	-78 dB
0	1	0	0	1	1	1	1	-79dB
x	1	1	x	x	x	x	x	mute

all other combinations not allowed

SUBADDRESS 8: Soft mute, Bass, Noise blanker time								
MSB							**LSB**	**FUNCTION**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
								Soft mute activation control
							0	I^2C bus Audio Processor mute ON (independently of pin Audio Mute)
							1	I^2C bus Audio Processor mute OFF (pin Audio Mute controls muting: pin=0 -> mute ON, pin=1 -> mute OFF)
					0	0		Soft mute transition time = 0.48 ms
					0	1		Soft mute transition time = 0.96 ms
					1	0		Soft mute transition time = 20.2 ms
					1	1		Soft mute transition time = 40.4 ms
								Bass filter center frequency
		0	0					60 Hz
		0	1					70 Hz
		1	0					80 Hz
		1	1					100 Hz (if bass DC mode OFF)
		1	1					150 Hz (if bass DC mode ON)
								Noise Blanker time
0	0							38 us
0	1							25.5 us
1	0							32 us
1	1							22 us

SUBADDRESS 9: Stereo decoder mute, st. dec. in-gain, mono, NB PEAK disch. Curr., pilot thresh., deemph.								
MSB							**LSB**	**FUNCTION**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
								Stereo Decoder Mute
							0	high-ohmic mute, pilot hold, multipath time constant short ENABLED (mute set by pin RDS mute LOW)
							1	high-ohmic mute, pilot hold, multipath time constant short DISABLED (regardless of pin RDS mute)
								Stereo Decoder In-gain
					1	1		0 dB
					1	0		2.5 dB
					0	1		4 dB
					0	0		5.5 dB
								Auto Zero Status
				0				disabled
				1				enabled; transition 0->1 performs Autozero sequence
								Force MONO
			0					ON
			1					OFF (automatic MONO/STEREO switch)
								Noiseblanker PEAK discharge current
		0						low
		1						high
								Pilot Threshold
	0							high
	1							low
								Deemphasis
0								50 us
1								75 us

SUBADDRESS 10: Noise blanker								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								Low threshold
					0	0	0	65 mV
					0	0	1	60 mV
					.	.	.	.
					1	1	1	30 mV
								Noise-controlled threshold
			0	0				320 mV
			0	1				260 mV
			1	0				200 mV
			1	1				140 mV
								Noise Blanker operation
		0						OFF
		1						ON
								Overdeviation adjustment
0	0							2.8 V
0	1							2.0 V
1	0							1.2 V
1	1							OFF

SUBADDRESS 11: High cut, multipath influence								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								High cut operation
							0	OFF
							1	ON
								Max. high cut
					0	0		2 dB
					0	1		5 dB
					1	0		7 dB
					1	1		10 dB
								VHCH
			0	0				42% REF 5V
			0	1				50% REF 5V
			1	0				58% REF 5V
			1	1				66% REF 5V
								VHCL
	0	0						16.7% VHCH
	0	1						22.2% VHCH
	1	0						27.8% VHCH
	1	1						33.3% VHCH
								Strong Multipath influence on PEAK 18k
0								OFF
1								ON (18k discharge if V_{MPOUT} < 2.5 V)

SUBADDRESS 12: Fieldstrength control								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								Noise blanker Field Strength Threshold
					0	0		min
					1	0		
					0	1		
					1	1		max
								Noise blanker Field Strength Gain
			0	0				2.3 V
			1	0				1.8 V
			0	1				1.3 V
			1	1				OFF
								Quality detector coefficient a
	0	0						a = 0.7
	0	1						a = 0.85
	1	0						a = 1.0
	1	1						a = 1.15
								Multipath influence on PEAK discharge
0								OFF
1								ON

SUBADDRESS 13: Noise rectifier disch. resistor, Multipath det. bandpass gain, multipath internal influence, reflection gain								
MSB							**LSB**	**FUNCTION**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
								Noise Rectifier Discharge Resistor
						0	0	R = infinite
						0	1	R = 56k
						1	0	R = 33k
						1	1	R = 18k
								Multipath Detector Bandpass Gain
				0	0			6 dB
				0	1			12 dB
				1	0			16 dB
				1	1			18 dB
								Multipath Detector Internal Influence
			0					ON
			1					OFF
								Multipath Detector Charge current
		0						0.5 uA
		1						1 uA
								Multipath Detector Reflection Gain
0	0							Gain = 7.6 dB
0	1							Gain = 4.6 dB
1	0							Gain = 0 dB
1	1							disabled

SUBADDRESS 14: Roll-off compensation, level gain								
MSB							**LSB**	**FUNCTION**
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
								Roll-off compensation
0					0	0	0	not allowed
0					0	0	1	7.2%
0					0	1	0	9.4%
.					.	.	.	.
0					1	0	0	13.7%
.					.	.	.	.
0					1	1	1	20.2%
1					0	0	0	not allowed
1					0	0	1	19.6%
1					0	1	0	21.5%
.					.	.	.	
1					1	0	0	25.3%
.					.	.	.	.
1					1	1	1	31.0%
								Level gain
	0	0	0	0				0 dB
	0	0	0	1				0.66 dB
	0	0	1	0				1.33 dB
	.	.	.	.				.
	1	1	1	1				10 dB

SUBADDRESS 15: TEST BYTE								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								Stereo Decoder test signals enabling
							0	test signal disabled
							1	test signal enabled (if S6=1) on ACinR
								Stereo Decoder test signals selection
		0	0	0	0			VHCCH
		0	0	0	1			LEVELINTERN
		0	0	1	0			PILOT
		0	0	1	1			VCOCON (VCO tuning voltage)
		0	1	0	0			PIL_VTH
		0	1	0	1			HOLDN
		0	1	1	0			NB_VTH
		0	1	1	1			F228
		1	0	0	0			VHCCL
		1	0	0	1			VSBL
		1	0	1	0			state machine enable ifc
		1	0	1	1			state machine set456
		1	1	0	0			PEAK
		1	1	0	1			state machine check
		1	1	1	0			REF5V
		1	1	1	1			SBPWM
								Test SC filters
						0		Fast test enabled (2-phase 200 kHz clock)
						1		Test disabled (4-phase 200 kHz clock)
								400 kHz VCO OFF
	0							OFF
	1							ON
								Audio processor test enabling
0								Test disabled
1								Test enabled (if S6 = 1)

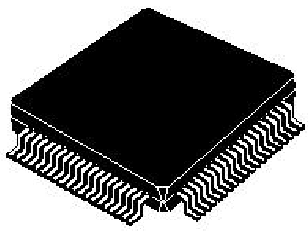
SUBADDRESS 16: Multipath test, AMHCC								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								Multipath test enable
							0	Multipath Detector test input disabled
							1	Multipath Detector test input enabled
								Quality detector noise gain
					0	0		15 dB
					0	1		12 dB
					1	0		9 dB
					1	1		6 dB
								AM High-cut control corner frequency
0	0	0	0	0				
0	0	0	0	1				
.	.	.	.	.				
1	1	1	1	0				
1	1	1	1	1				

SUBADDRESS 17: Mid								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								Mid Filter steps
			0	0	0	0	0	-15 dB
			0	0	0	0	1	-14 dB
			.	.	.	.	.	.
			0	1	1	1	0	-1 dB
			0	1	1	1	1	0 dB
			1	1	1	1	1	0 dB
			1	1	1	1	0	+1 dB
			.	.	.	.	.	.
			1	0	0	0	1	+14 dB
			1	0	0	0	0	+15 dB
								Mid Filter center frequency
	0	0						500 Hz
	0	1						1.0 kHz
	1	0						1.5 kHz
	1	1						2.0 kHz
								Mid Filter Q factor
0								1.0
1								2.0

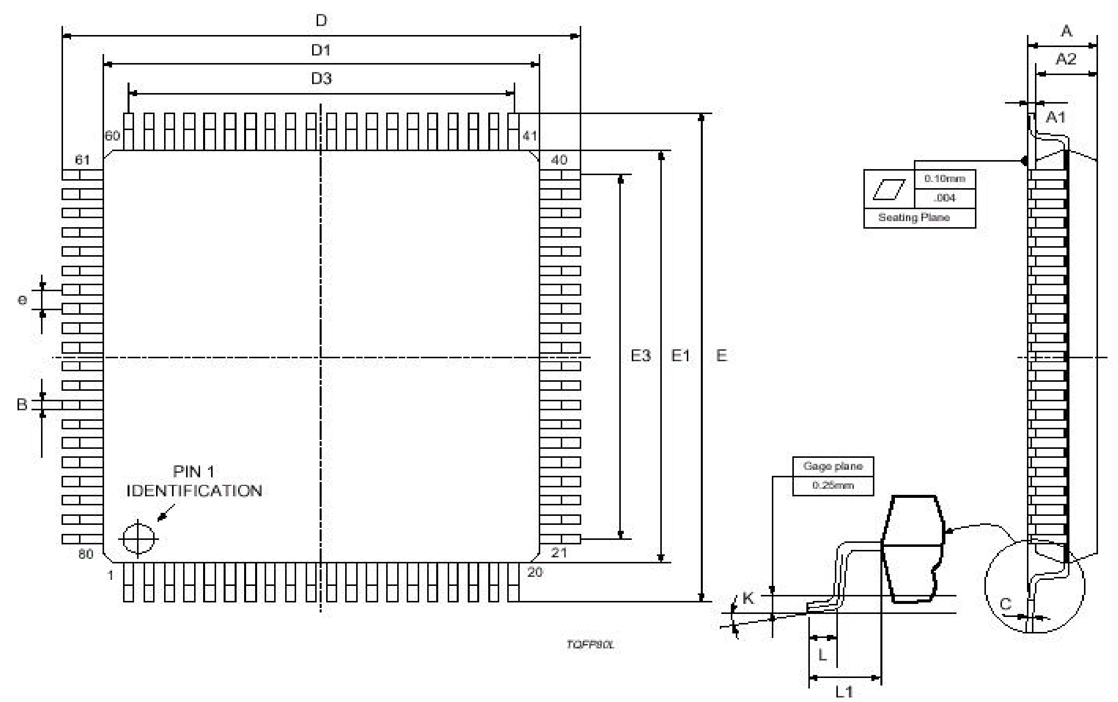
SUBADDRESS 18: Stereo blend								
MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								VSBL
					0	0	0	VSBL at 29% REF 5V
					0	0	1	VSBL at 33% REF 5V
					0	1	0	VSBL at 38% REF 5V
					0	1	1	VSBL at 42% REF 5V
					1	0	0	VSBL at 46% REF 5V
					1	0	1	VSBL at 50% REF 5V
					1	1	0	VSBL at 54% REF 5V
					1	1	1	VSBL at 58% REF 5V

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.22	0.32	0.38	0.009	0.013	0.015
C	0.09		0.20	0.003		0.008
D		16.00			0.630	
D1		14.00			0.551	
D3		12.35			0.295	
e		0.65			0.0256	
E		16.00			0.630	
E1		14.00			0.551	
E3		12.35			0.486	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.0393	
K	3.5°(min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



TQFP80 (14x14x1.40mm)



May 1998

0062342